7534 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0099-0300
Rev.3.00
Oct 23, 2006

DESCRIPTION

The 7534 Group is the 8-bit microcomputer based on the 740 family core technology.
The 7534 Group has a USB, 8-bit timers, and an A/D converter, and is useful for an input device for personal computer peripherals.

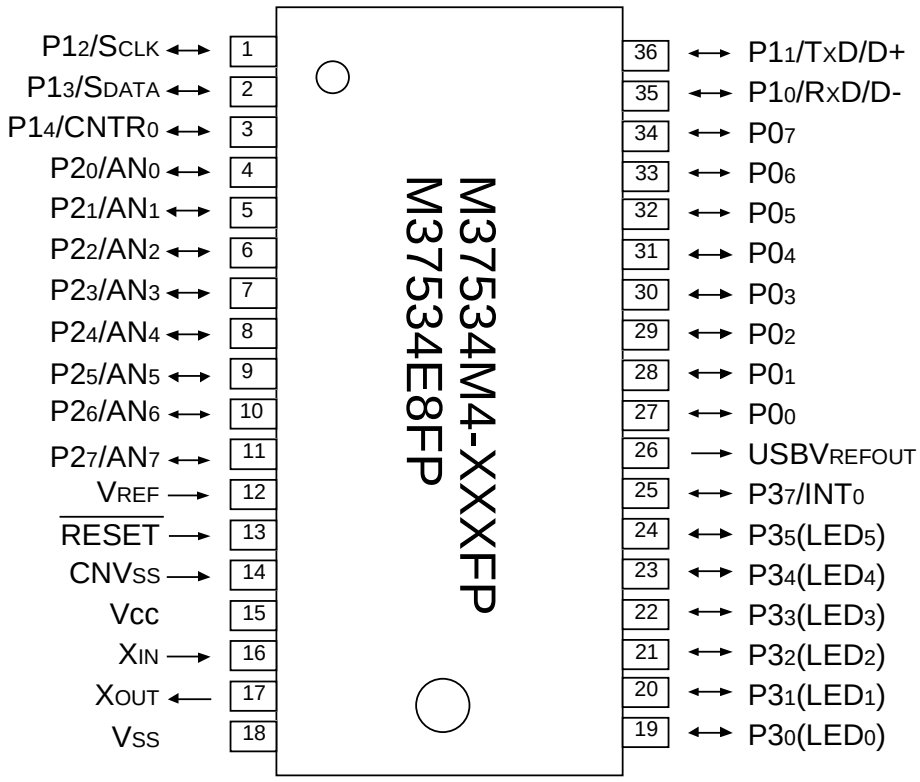
FEATURES

- Basic machine-language instructions 69
- The minimum instruction execution time ..... 0.34 µs
  (at 6 MHz oscillation frequency for the shortest instruction)
- Memory size
  ROM ..... 8K to 16K bytes
  RAM ..... 256 to 384 bytes
- Programmable I/O ports ..... 28 (36-pin type)
  ..... 24 (32-pin type)
  ..... 33 (42-pin type)
- Interrupts ..... 14 sources, 8 vectors
- Timers ..... 8-bit × 3
- Serial Interface
  Serial I/O1 ..... used only for Low Speed in USB (based on Low-Speed USB2.0 specification) (USB/UART)
  Serial I/O2 ..... 8-bit × 1 (Clock-synchronized)
- A/D converter ..... 10-bit × 8 channels
- Clock generating circuit ..... Built-in type
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  At 6 MHz X_{IN} oscillation frequency at ceramic resonator
  ..... 4.1 to 5.5 V(4.4 to 5.25 V at USB operation)
- Power dissipation ..... 30 mW (standard)
- Operating temperature range ..... –20 to 85 °C
  (0 to 70 °C at USB operation)
- Built-in USB 3.3 V Regulator + transceiver based on Low-Speed USB2.0 specification

APPLICATION

Input device for personal computer peripherals

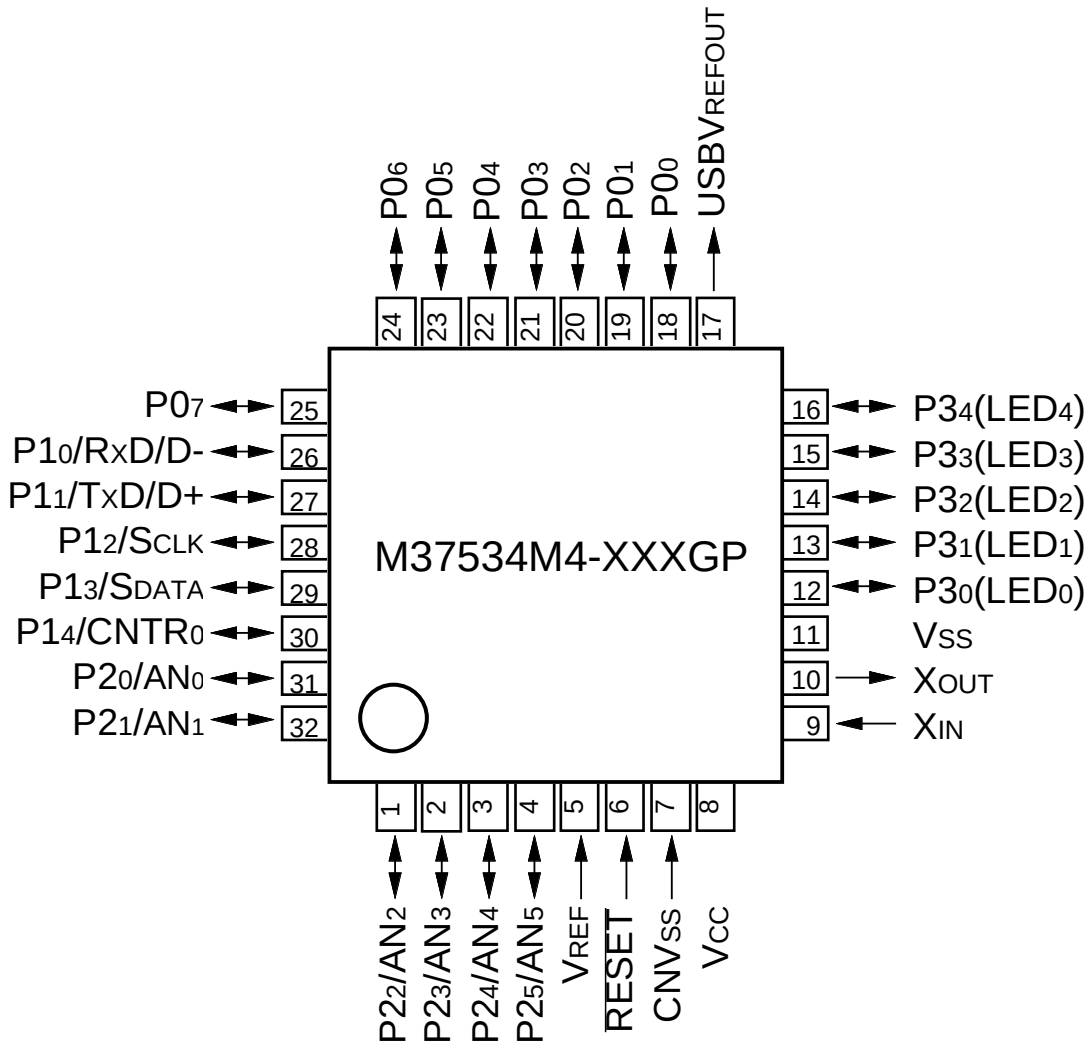
PIN CONFIGURATION (TOP VIEW)



Package type: PRSP0036GA-A (36P2R-A)

Fig. 1 Pin configuration of M37534M4-XXXFP, M37534E8FP

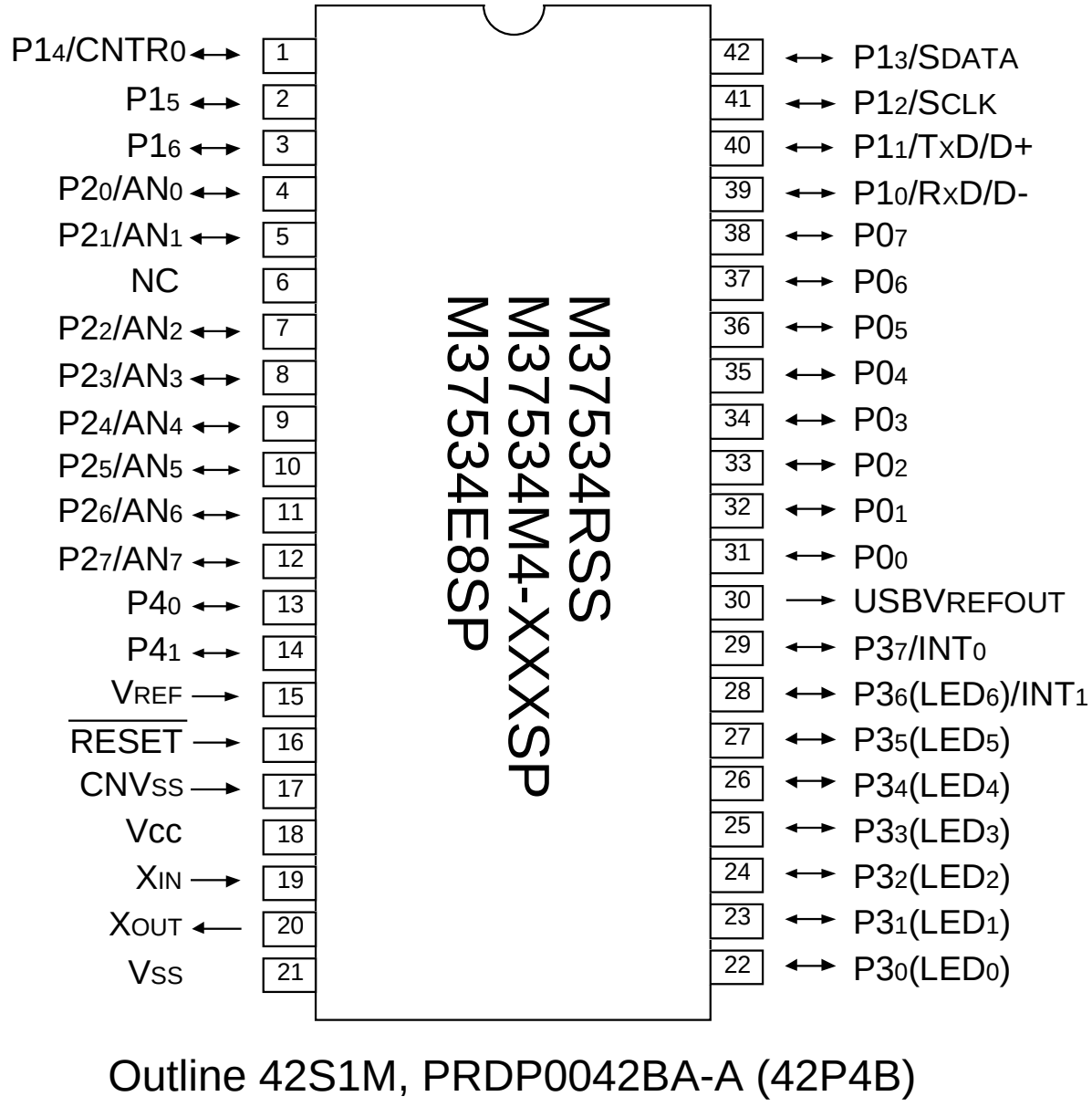
PIN CONFIGURATION (TOP VIEW)



Outline PLQP0032GB-A (32P6U-A)

Fig. 2 Pin configuration of M37534M4-XXXGP

PIN CONFIGURATION (TOP VIEW)



Outline 42S1M, PRDP0042BA-A (42P4B)

Fig. 3 Pin configuration of M37534RSS, M37534M4-XXXSP, M37534E8SP

FUNCTIONAL BLOCK

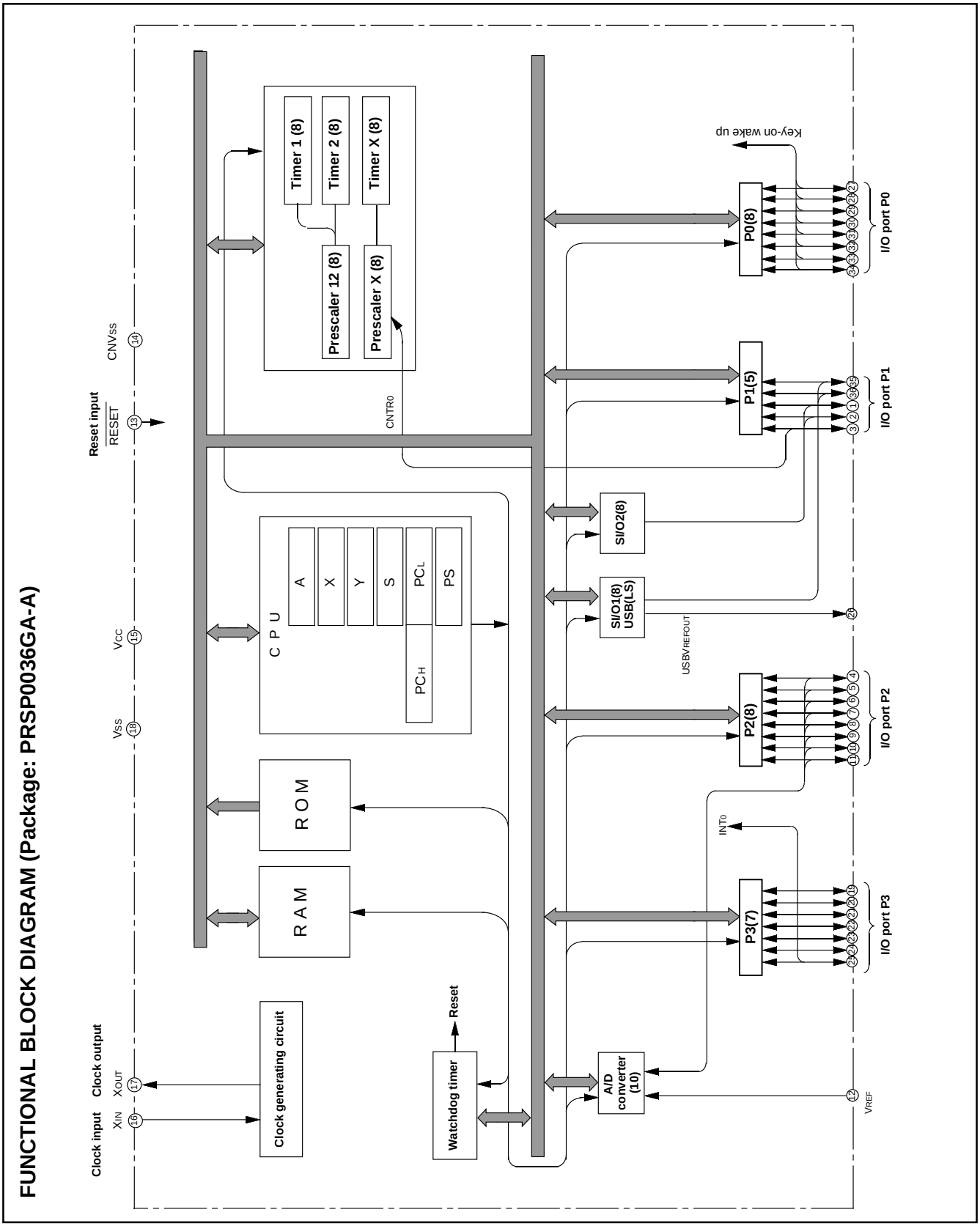


Fig. 4 Functional block diagram (PRSP0036GA-A package type)

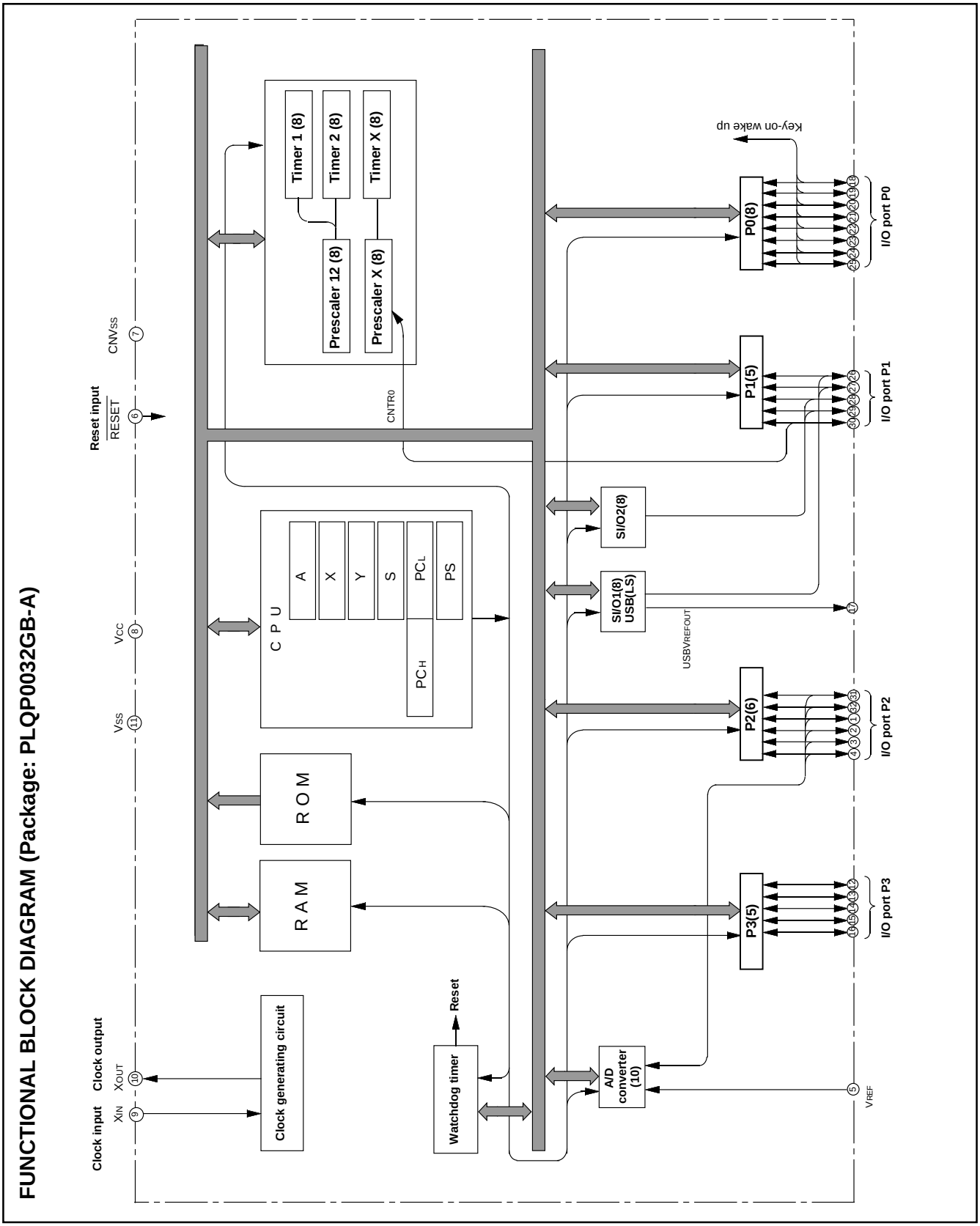


Fig. 5 Functional block diagram (PLQP0032GB-A package type)

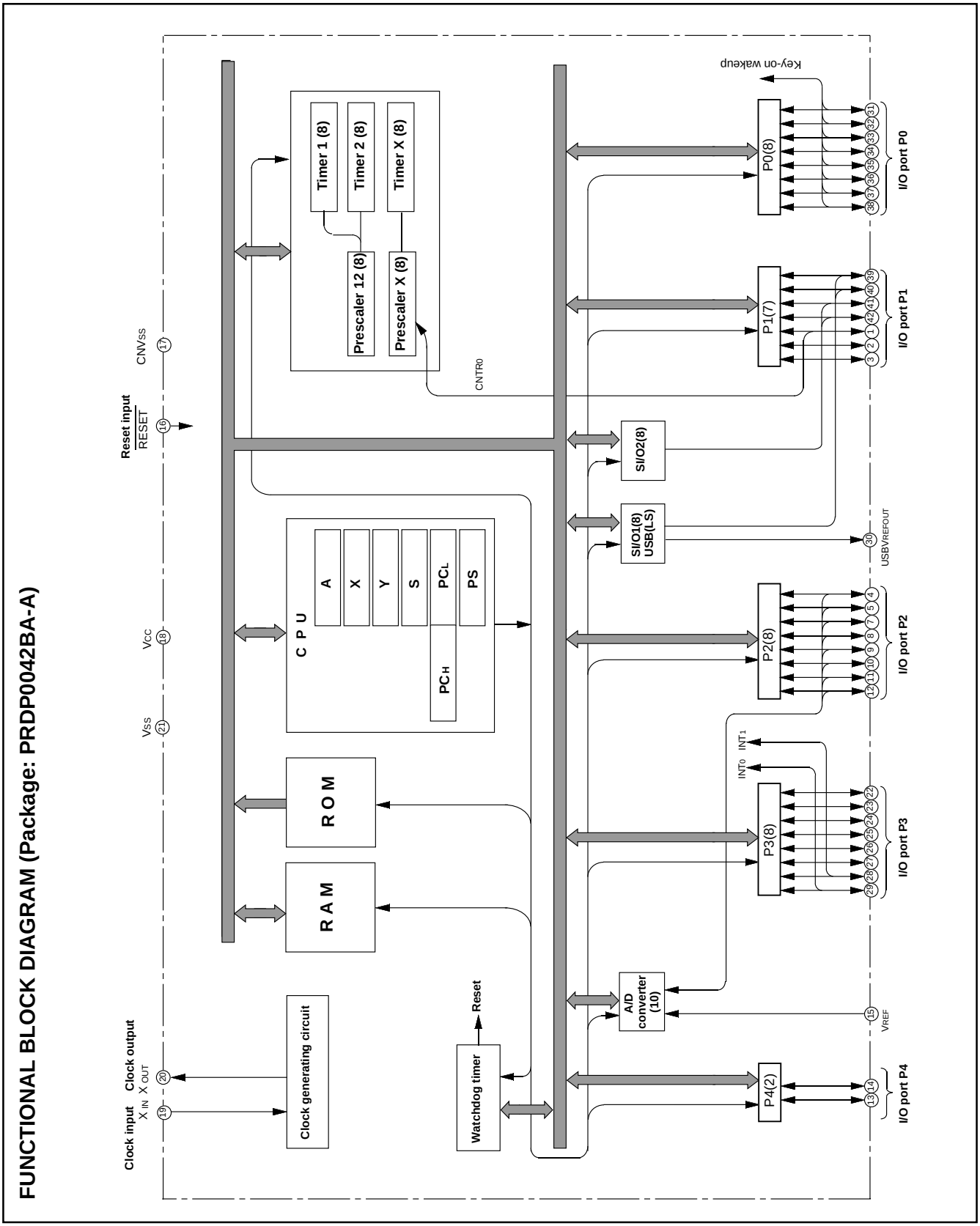


Fig. 6 Functional block diagram (PRDP0042BA-A package type)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source	•Apply voltage of 4.1 to 5.5 V (4.4 to 5.25 V at USB operating) to Vcc, and 0 V to Vss.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A/D converter	
USBV_{REFOUT}	USB reference voltage output	•Output pin for pulling up a D- line with 1.5 kΩ external resistor	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L”	
X_{IN}	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz crystal oscillator between the X_{IN} and X_{OUT} pins. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Key-input (key-on wake up interrupt input) pins
$P1_0$/RxD/D- $P1_1$/TxD/D+	I/O port P1	•7-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for $P1_0$, $P1_2$, $P1_3$. •When using the USB function, input level of ports $P1_0$ and $P1_1$ becomes USB input level, and output level of them becomes USB output level.	•Serial I/O1 function pin
$P1_2$/S_{CLK} $P1_3$/S_{DATA}			•Serial I/O2 function pin
$P1_4$/$CNTR_0$			•Timer X function pin
$P1_5$, $P1_6$			
$P2_0$/AN_0– $P2_7$/AN_7	I/O port P2	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	•Input pins for A/D converter
$P3_0$–$P3_5$	I/O port P3	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for $P3_6$, $P3_7$). •CMOS 3-state output structure •$P3_0$ to $P3_6$ can output a large current for driving LED.	
$P3_6$/INT_1 $P3_7$/INT_0		•Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Interrupt input pins
$P4_0$, $P4_1$	I/O port P4	•2-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output.	

GROUP EXPANSION

Renesas expands the 7534 group as follow:

Memory type

Support for Mask ROM version, One Time PROM version, and Emulator MCU .

Memory size

ROM/PROM size ..... 8 K to 16 K bytes
RAM size ..... 256 to 384 bytes

Package

PRSP0036GA-A ..... 0.8 mm-pitch plastic molded SOP
PLQP0032GB-A ..... 0.8 mm-pitch plastic molded LQFP
PRDP0042BA-A ..... 42 pin plastic molded SDIP
42SIM ..... 42 pin shrink ceramic PIGGY BACK

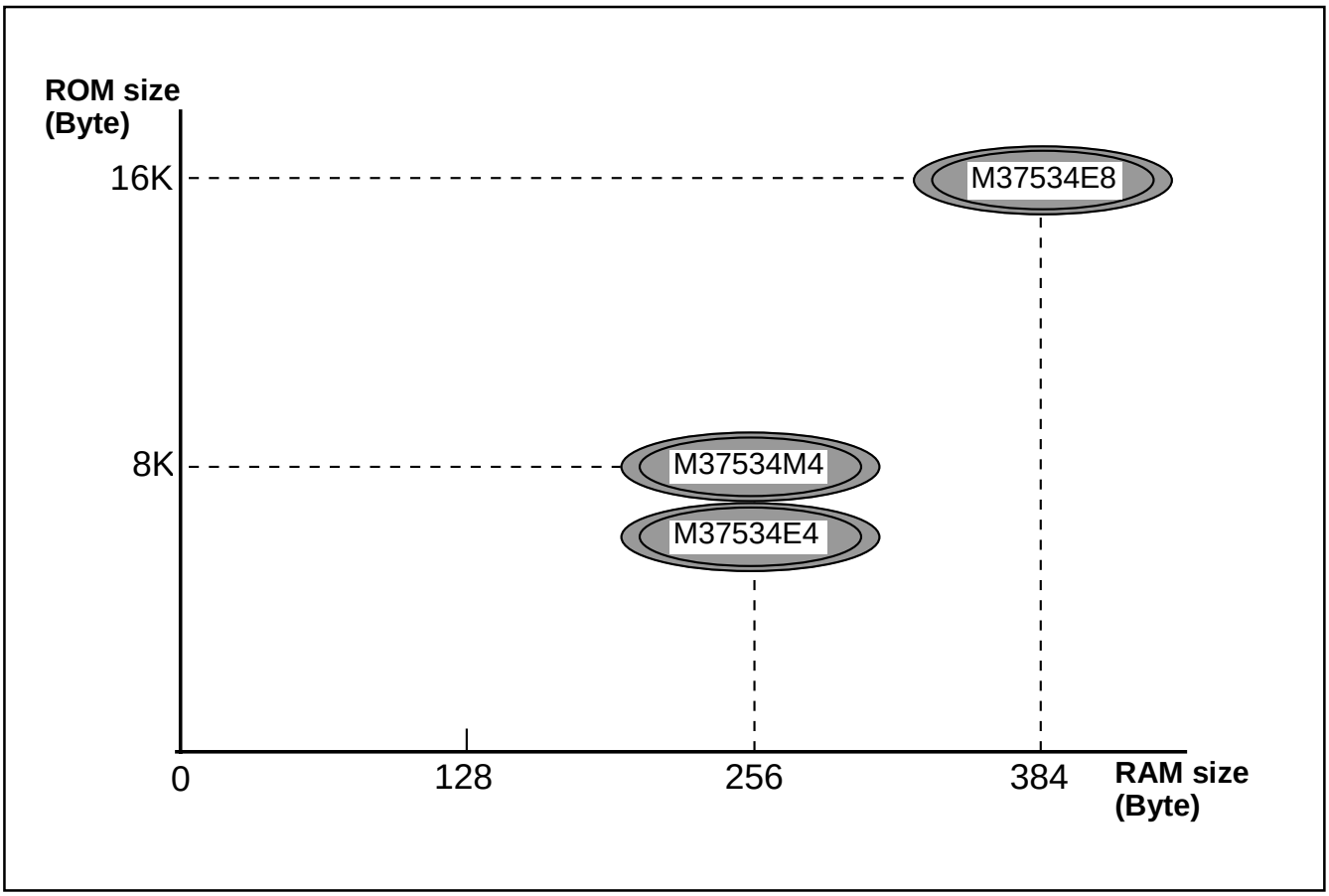


Fig. 7 Memory expansion

Currently supported products are listed below.

Table 2 List of supported products

Part number	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37534M4-XXXFP	8192 (8062)	256	PRSP0036GA-A	Mask ROM version
M37534M4-XXXGP	8192 (8062)	256	PLQP0032GB-A	Mask ROM version
M37534M4-XXXSP	8192 (8062)	256	PRDP0042BA-A	Mask ROM version
M37534E4GP	8192 (8062)	256	PLQP0032GB-A	One Time PROM version (blank)
M37534E8FP	16384 (16254)	384	PRSP0036GA-A	One Time PROM version (blank)
M37534E8SP	16384 (16254)	384	PRDP0042BA-A	One Time PROM version (blank)
M37534RSS	————	384	42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 7534 Group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the 740 Family Software Manual for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions cannot be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

[CPU Mode Register] CPUM

The CPU mode register contains the stack page selection bit. This register is allocated at address $003B_{16}$.

Note on stack page

When 1 page is used as stack area by the stack page selection bit, the area which can be used as stack depends on RAM size. Especially, be careful that the RAM area varies in Mask ROM version, One Time PROM version and Emulator MCU.

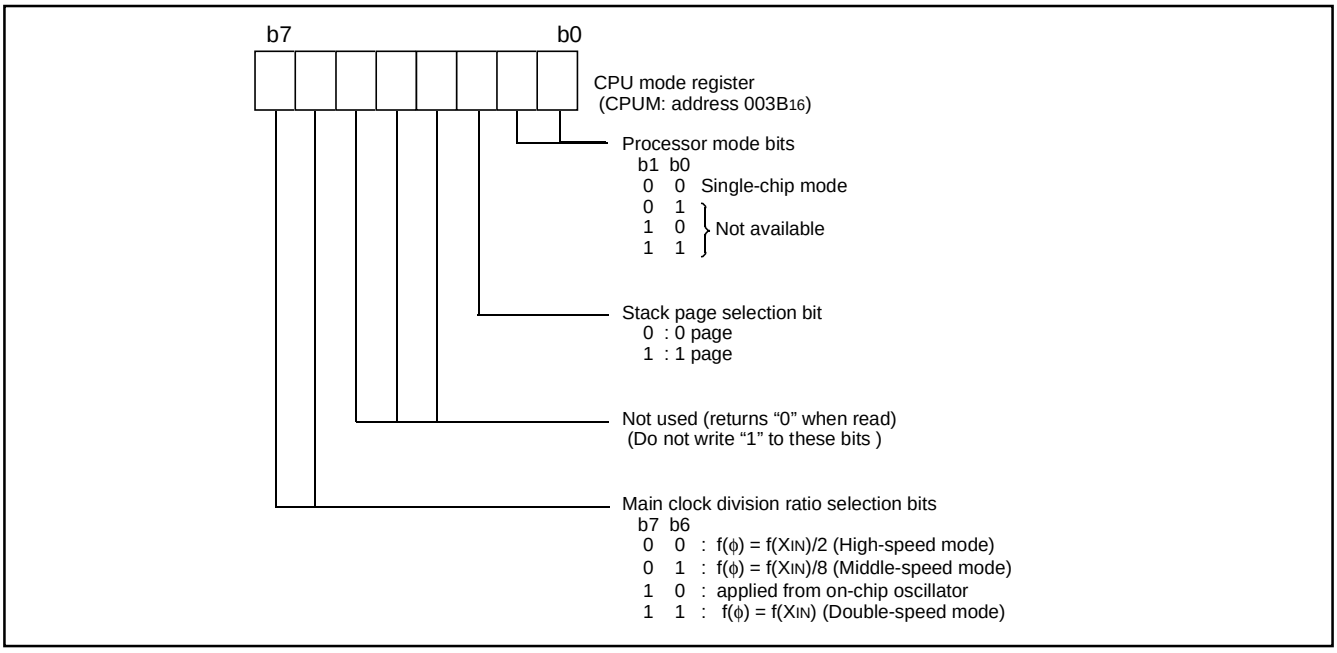


Fig. 8 Structure of CPU mode register

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

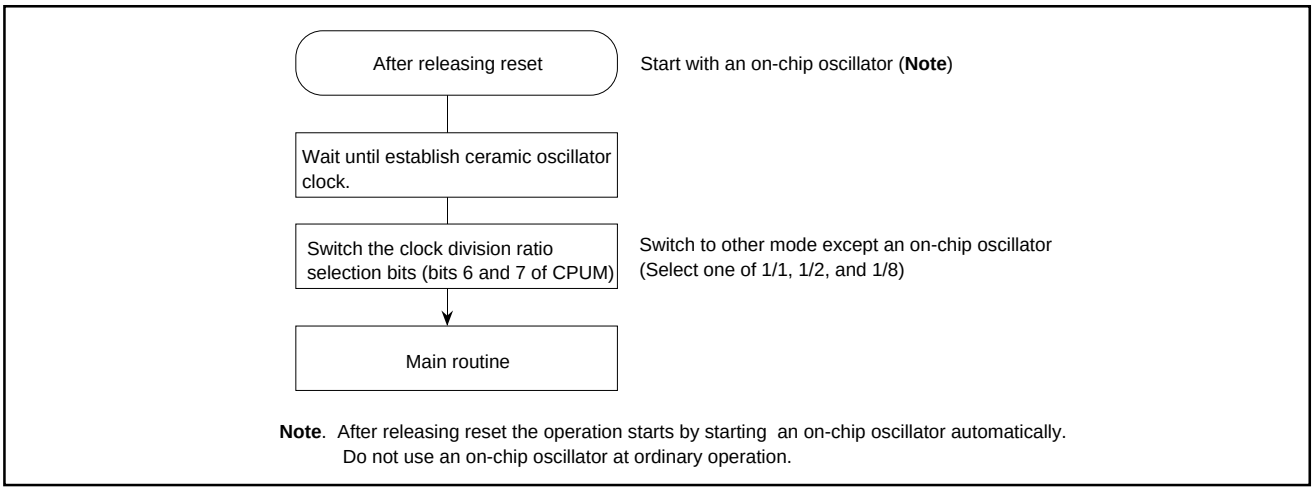


Fig. 9 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

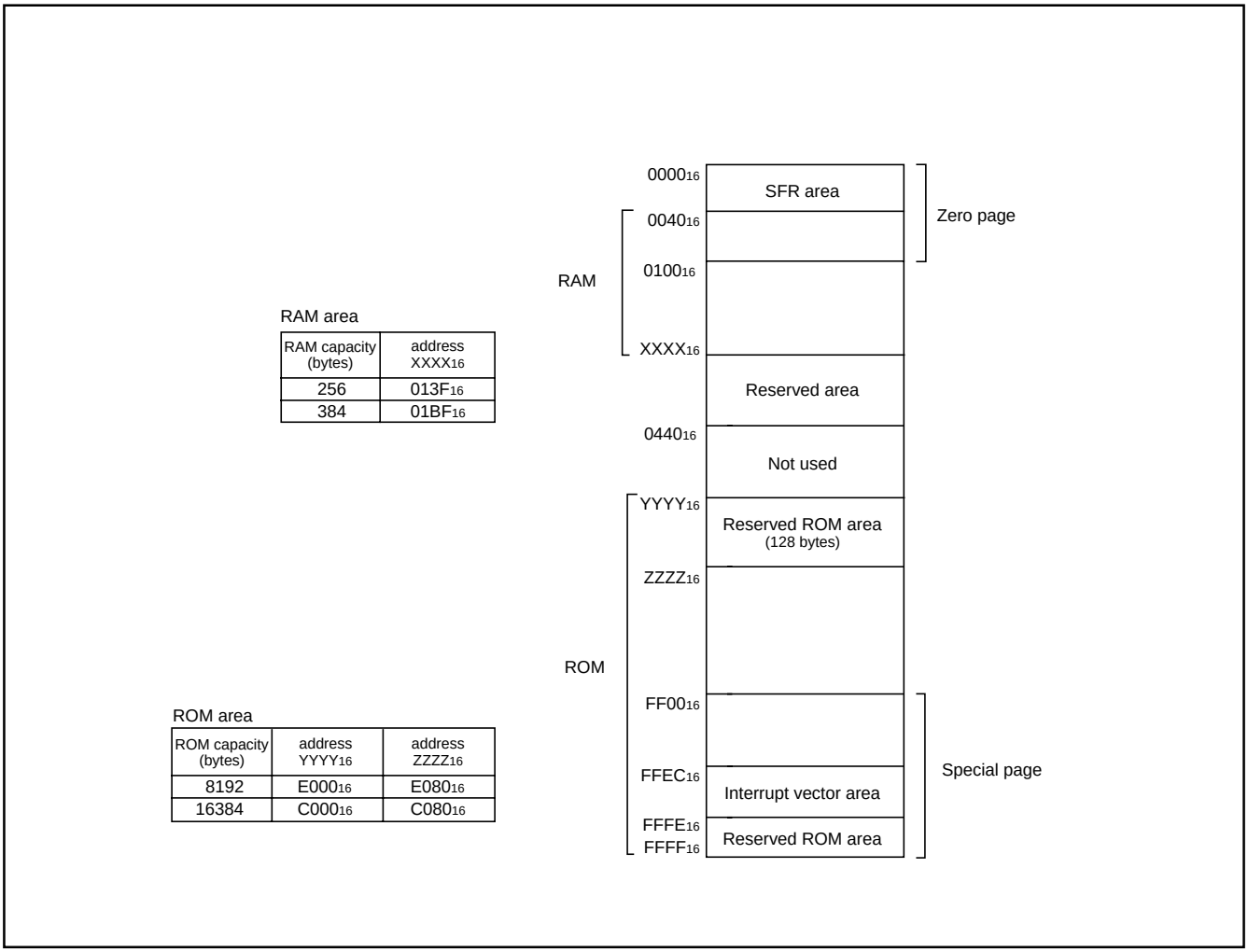


Fig. 10 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	USB interrupt control register (USBICON)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	USB transmit data byte number set register 0 (EP0BYTE)
0002_{16}	Port P1 (P1)	0022_{16}	USB transmit data byte number set register 1 (EP1BYTE)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	USBPID control register 0 (EP0PID)
0004_{16}	Port P2 (P2)	0024_{16}	USBPID control register 1 (EP1PID)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	USB address register (USBA)
0006_{16}	Port P3 (P3)	0026_{16}	USB sequence bit initialization register (INISQ1)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	USB control register (USBCON)
0008_{16}	Port P4 (P4)	0028_{16}	Prescaler 12 (PRE12)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 1 (T1)
$000A_{16}$		$002A_{16}$	Timer 2 (T2)
$000B_{16}$		$002B_{16}$	Timer X mode register (TM)
$000C_{16}$		$002C_{16}$	Prescaler X (PREX)
$000D_{16}$		$002D_{16}$	Timer X (TX)
$000E_{16}$		$002E_{16}$	Timer count source set register (TCSS)
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}		0031_{16}	Serial I/O2 register (SIO2)
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A/D control register (ADCON)
0015_{16}		0035_{16}	A/D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A/D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	USB status register (USBSTS)/UART status register (UARTSTS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	USB data toggle synchronization register (TRSYNC)	$003D_{16}$	
$001E_{16}$	USB interrupt source discrimination register 1 (USBIR1)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	USB interrupt source discrimination register 2 (USBIR2)	$003F_{16}$	

Fig. 11 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port. When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control] PULL

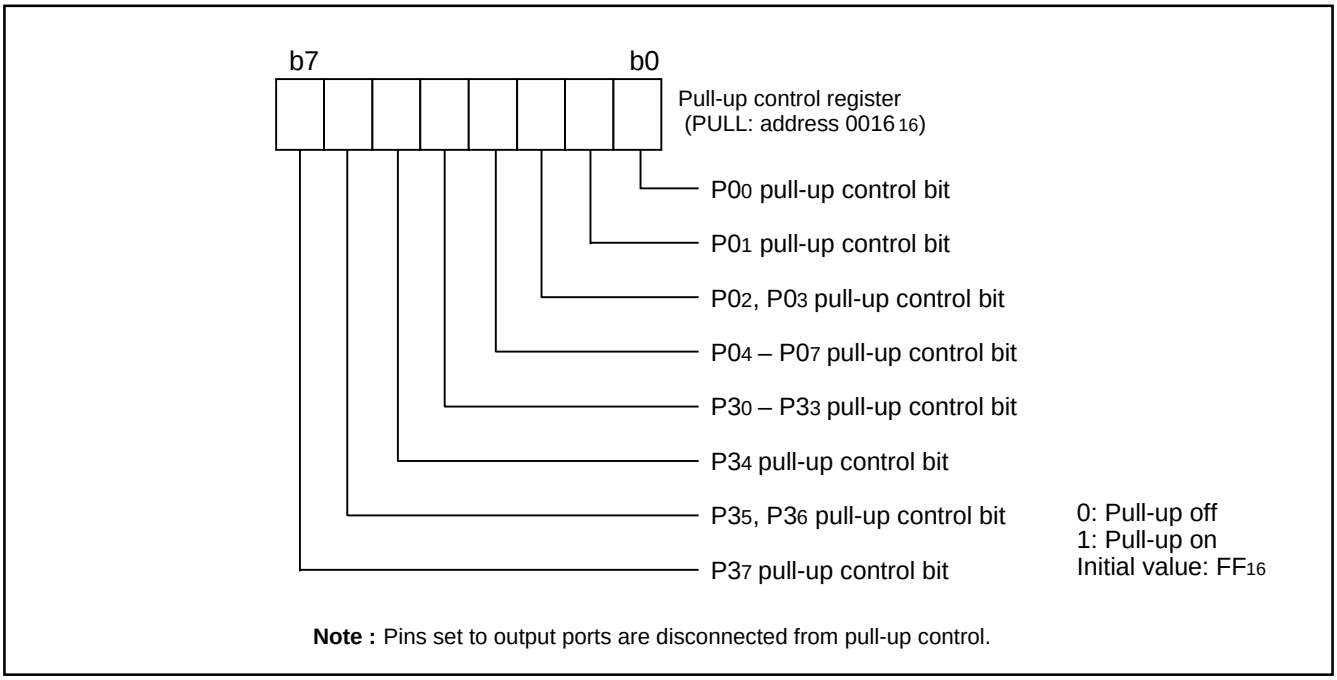
By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P1_3$, $P3_6$ and $P3_7$ by program.

Then, as for the 36-pin version, set "1" to each bit 6 of the port P3 direction register and port P3 register.

As for the 32-pin version, set "1" to respective bits 5, 6, 7 of the port P3 direction register and port P3 register.



Note : Pins set to output ports are disconnected from pull-up control.

Fig. 12 Structure of pull-up control register

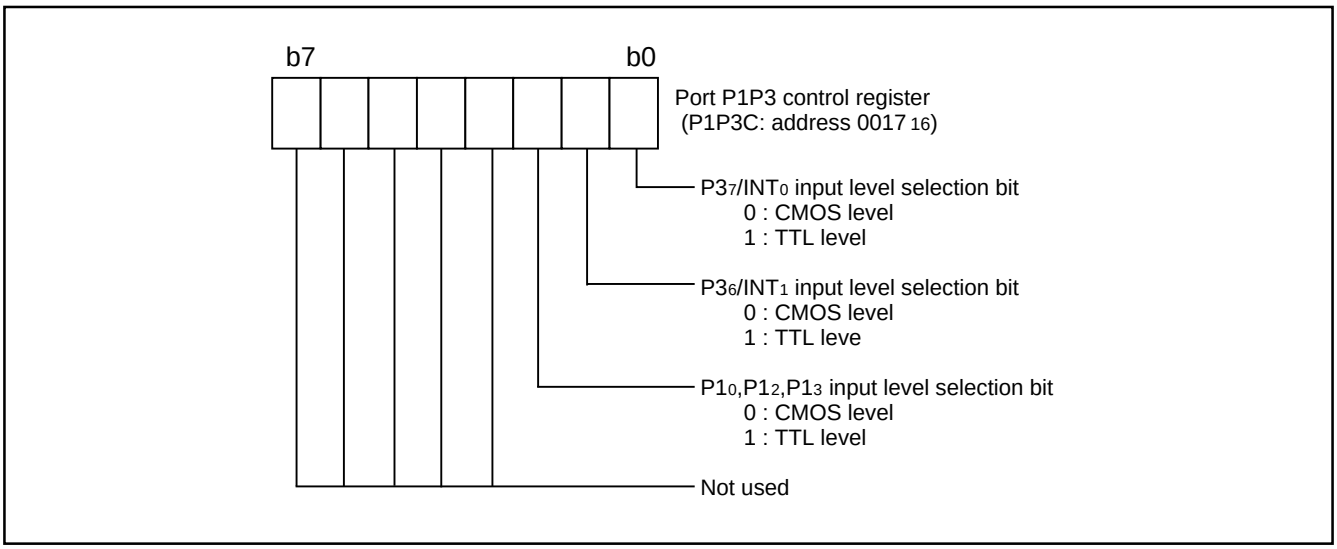
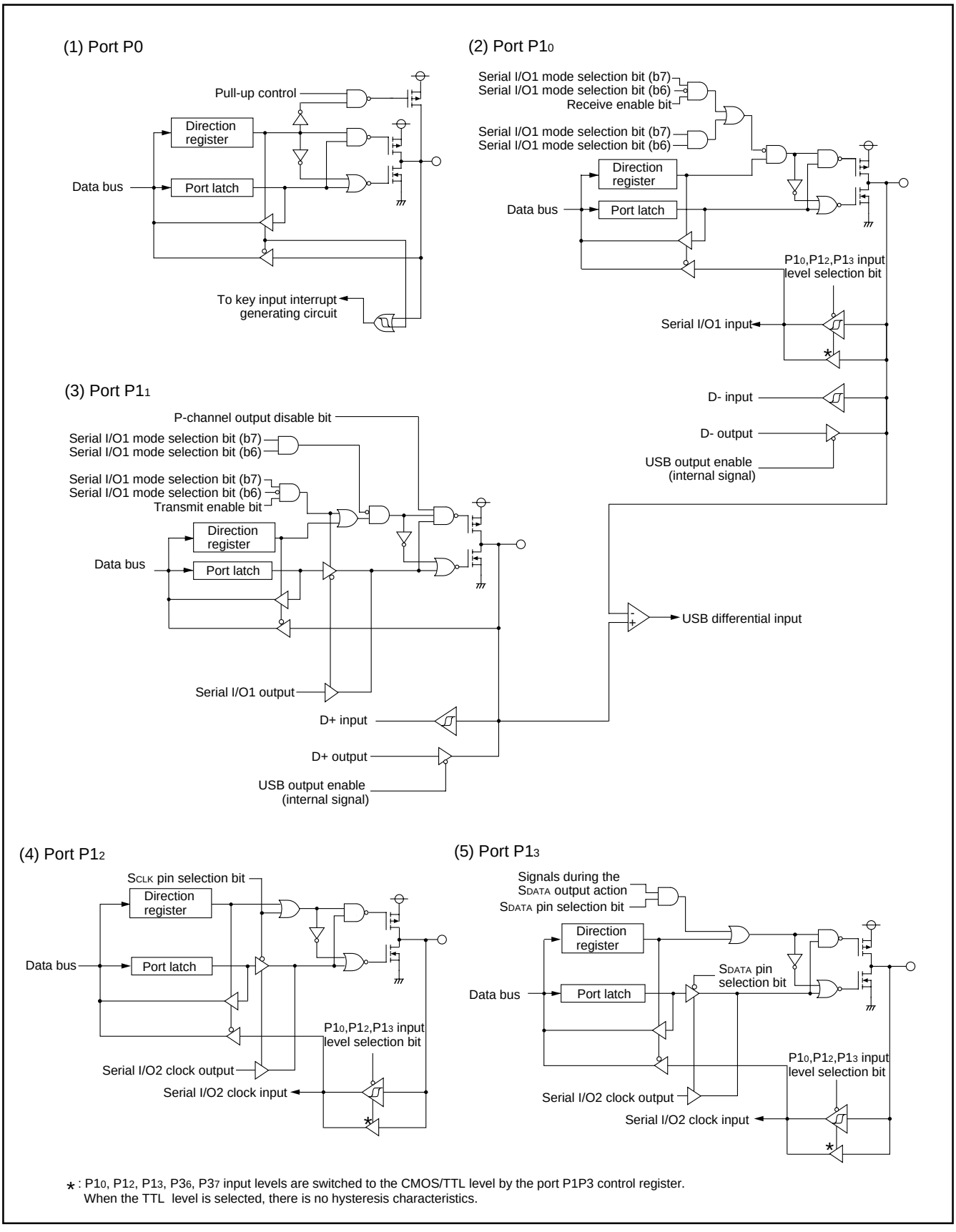


Fig. 13 Structure of port P1P3 control register

Table 3 I/O port function table

Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
$P0_0$–$P0_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output	Key input interrupt	Pull-up control register	(1)
$P1_0$/RxD/D- $P1_1$/TxD/D+	I/O port P1		•USB input/output level when selecting USB function	Serial I/O1 function input/ output	Serial I/O1 control register	(2) (3)
$P1_2$/SCLK $P1_3$/SDATA			•CMOS compatible input level •CMOS 3-state output (Note)	Serial I/O2 function input/ output	Serial I/O2 control register	(4) (5)
$P1_4$/$CNTR_0$				Timer X function input/output	Timer X mode register	(6)
$P1_5$, $P1_6$						(10)
$P2_0$/AN_0– $P2_7$/AN_7	I/O port P2			A/D conversion input	A/D control register	(7)
$P3_0$–$P3_5$	I/O port P3					(8)
$P3_6$/INT_1 $P3_7$/INT_0				External interrupt input	Interrupt edge selection register	(9)
$P4_0$, $P4_1$	I/O port P4					(10)

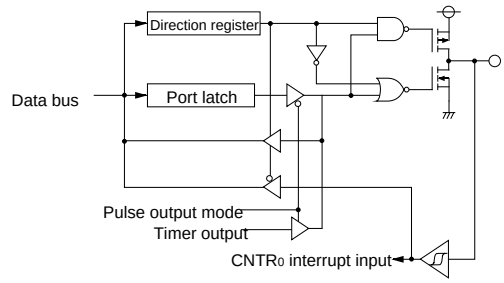
Note: Port $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ is CMOS/TTL level.



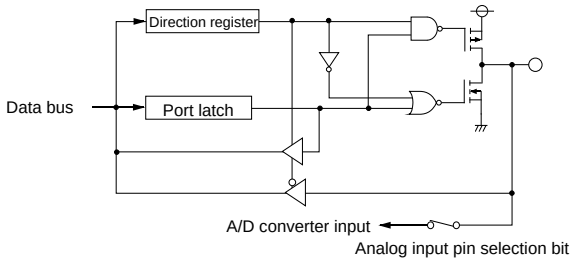
* : P10, P12, P13, P36, P37 input levels are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 14 Block diagram of ports (1)

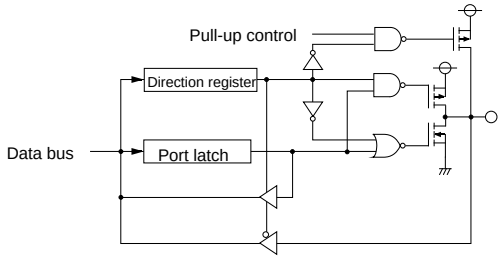
(6) Ports $P1_4$



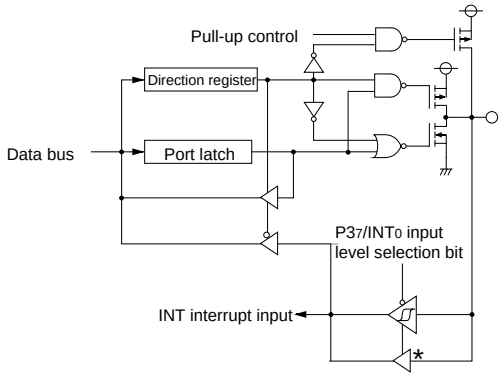
(7) Ports $P2_0$–$P2_7$



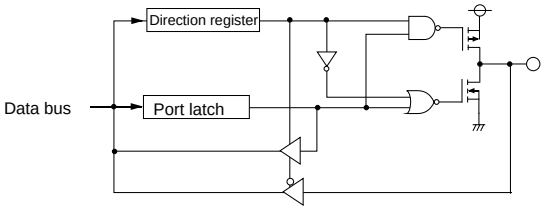
(8) Ports $P3_0$–$P3_5$



(9) Ports $P3_6$, $P3_7$



(10) Ports $P1_5$, $P1_6$, $P4_0$, $P4_1$



*: $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ input levels are switched to the CMOS/TTL level by the port P1P3 control register. When the TTL level is selected, there is no hysteresis characteristics.

Fig. 15 Block diagram of ports (2)

Interrupts

Interrupts occur by 14 different sources : 4 external sources, 9 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to “1” and the interrupt disable flag is set to “0”, an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set. The interrupt enable bit can be set and cleared by program.

It becomes usable by switching $CNTR_0$ and A/D interrupt sources with bit 7 of the interrupt edge selection register, timer 2 and serial I/O2 interrupt sources with bit 6, timer X and key-on wake-up interrupt sources with bit 5, and serial I/O transmit and INT_1 interrupt sources with bit 4.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT_0, INT_1, $CNTR_0$) is set, the interrupt request bit may be set.

Therefore, please take following sequence:

1. Disable the external interrupt which is selected.
2. Change the active edge in interrupt edge selection register. (in case of $CNTR_0$: Timer X mode register)
3. Clear the set interrupt request bit to “0”.
4. Enable the external interrupt which is selected.

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
UART receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of UART data receive	Valid in UART mode
USB IN token				At detection of IN token	Valid in USB mode
UART transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of UART transmit shift or when transmit buffer is empty	Valid in UART mode
USB SETUP/OUT token Reset/Suspend/Resume				At detection of SETUP/OUT token or At detection of Reset/ Suspend/ Resume	Valid in USB mode
INT_1				At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Timer X	5	$FFF5_{16}$	$FFF4_{16}$	At timer X underflow	
Key-on wake-up				At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
Timer 1	6	$FFF3_{16}$	$FFF2_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	7	$FFF1_{16}$	$FFF0_{16}$	At timer 2 underflow	
Serial I/O2				At completion of transmit/receive shift	
$CNTR_0$	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
A/D conversion				At completion of A/D conversion	
BRK instruction	9	$FFED_{16}$	$FFEC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

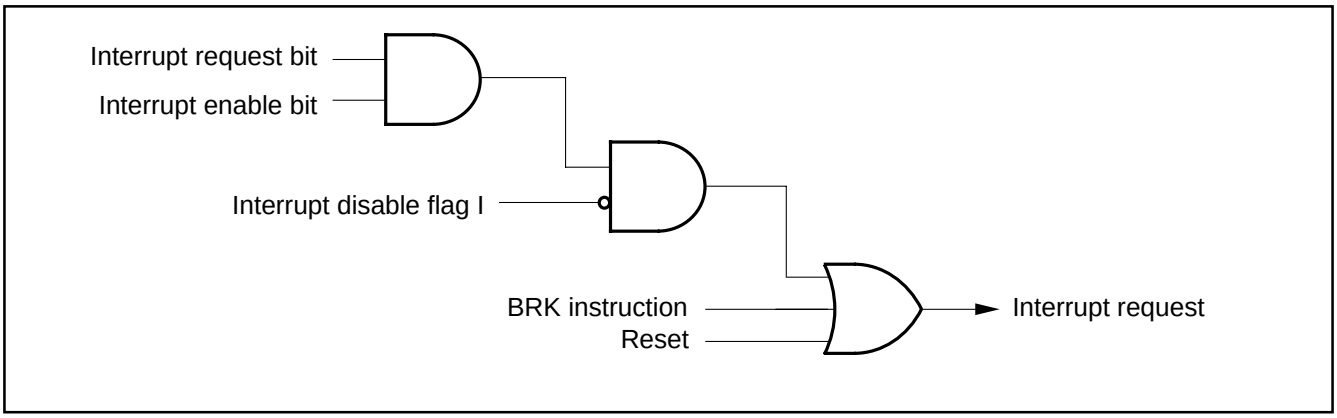


Fig. 16 Interrupt control

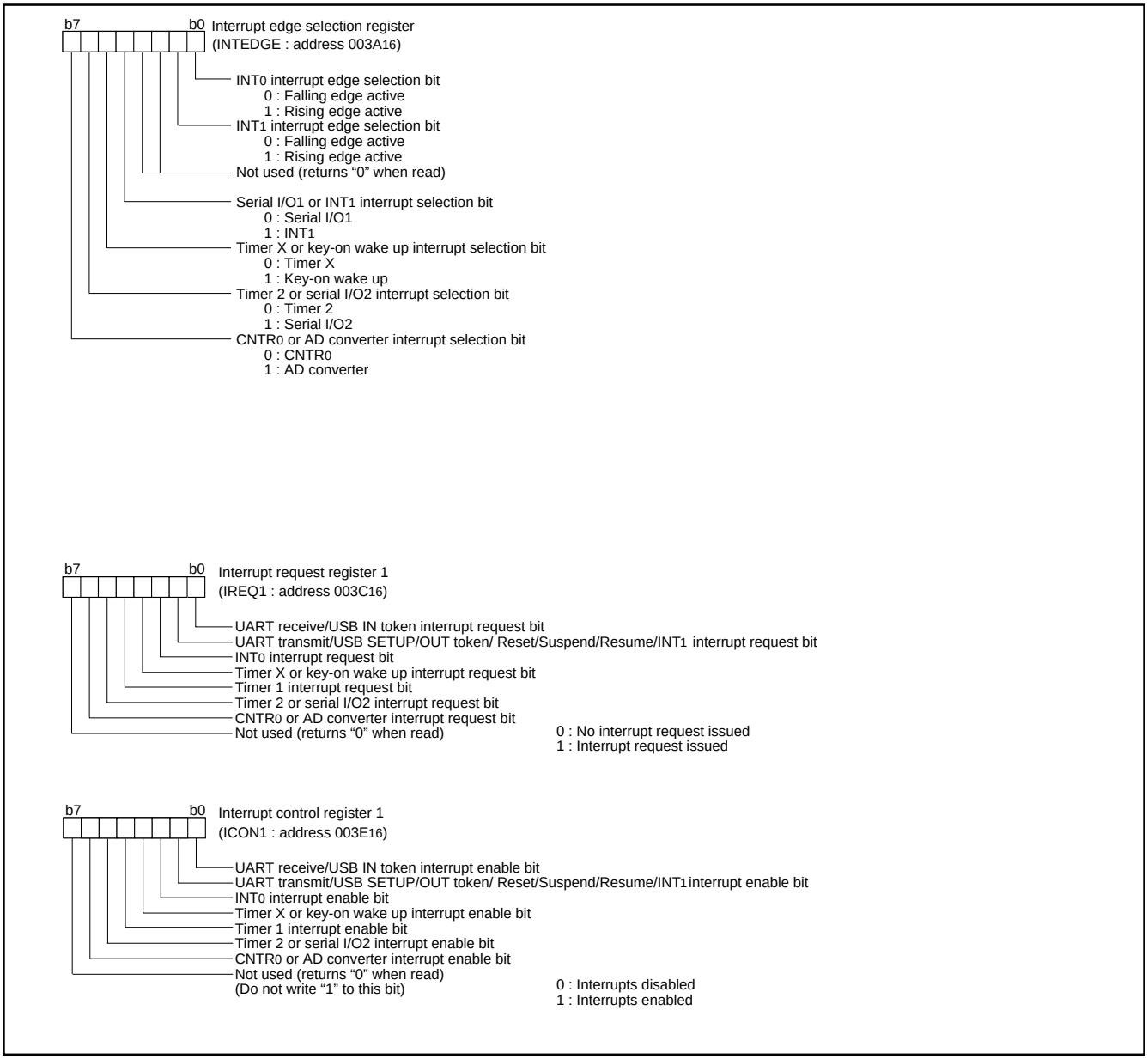


Fig. 17 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying “L” level to any pin of port P0 that has been set to input mode.
In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports $P0_0$ to $P0_3$ as input ports.

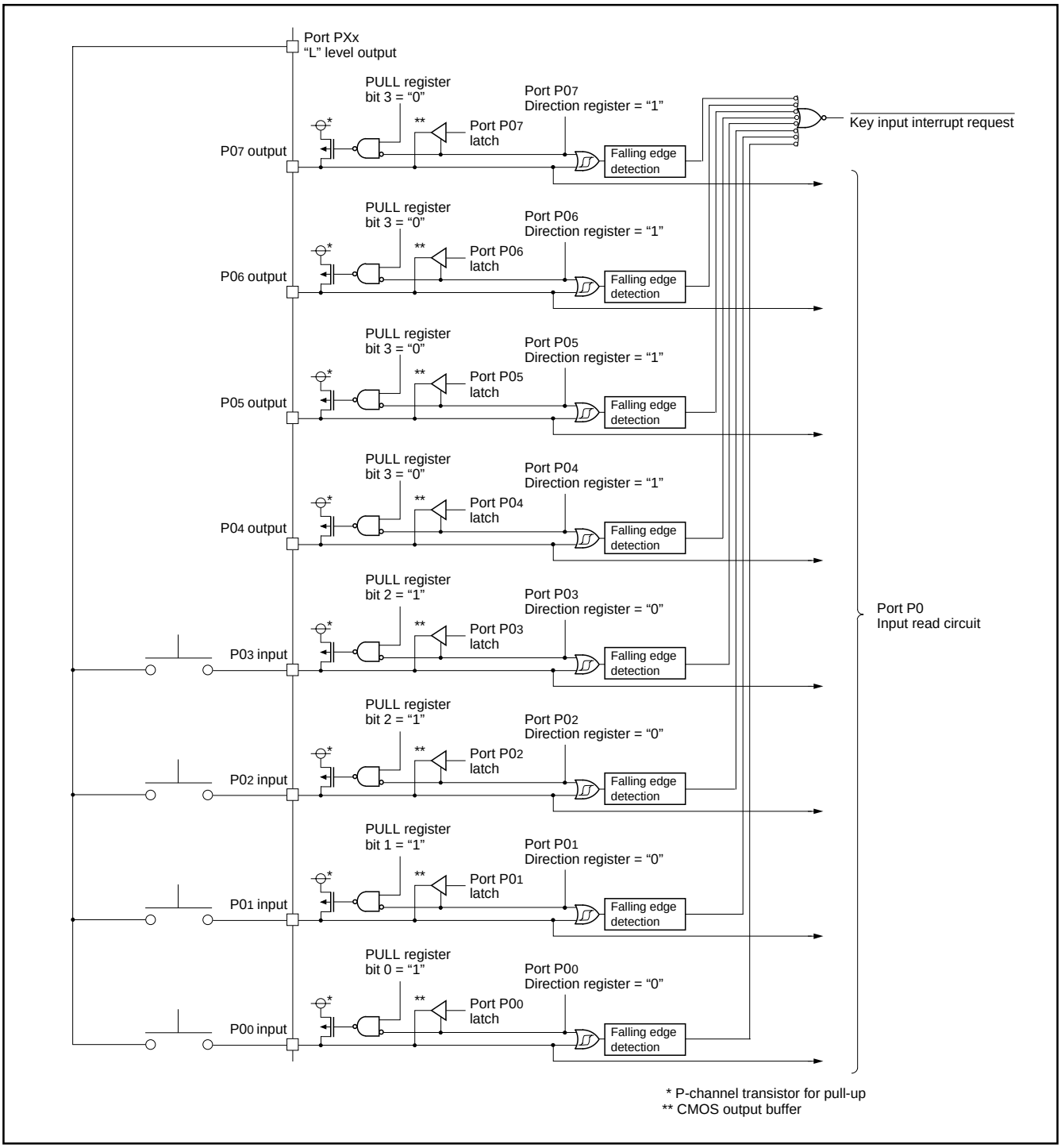


Fig. 18 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7534 Group has 3 timers: timer X, timer 1 and timer 2.

The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.

All the timers are down count timers. When a timer reaches “0”, an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to “1”.

●Timer 1, Timer 2

Prescaler 12 always counts f(XIN)/16. Timer 1 and timer 2 always count the prescaler output and periodically sets the interrupt request bit.

●Timer X

Timer X can be selected in one of 4 operating modes by setting the timer X mode register.

• Timer Mode

The timer counts the signal selected by the timer X count source selection bit.

• Pulse Output Mode

The timer counts the signal selected by the timer X count source selection bit, and outputs a signal whose polarity is inverted each time the timer value reaches “0”, from the CNTR0 pin.

When the CNTR0 active edge switch bit is “0”, the output of the CNTR0 pin is started with an “H” output.

At “1”, this output is started with an “L” output. When using a timer in this mode, set the port P14 direction register to output mode.

• Event Counter Mode

The operation in the event counter mode is the same as that in the timer mode except that the timer counts the input signal from the CNTR0 pin.

When the CNTR0 active edge switch bit is “0”, the timer counts the rising edge of the CNTR0 pin. When this bit is “1”, the timer counts the falling edge of the CNTR0 pin.

• Pulse Width Measurement Mode

When the CNTR0 active edge switch bit is “0”, the timer counts the signal selected by the timer X count source selection bit while the CNTR0 pin is “H”. When this bit is “1”, the timer counts the signal while the CNTR0 pin is “L”.

In any mode, the timer count can be stopped by setting the timer X count stop bit to “1”. Each time the timer overflows, the interrupt request bit is set.

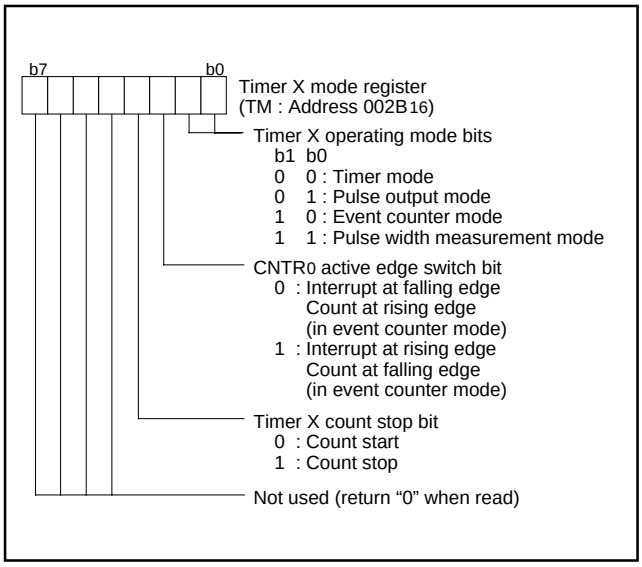


Fig. 19 Structure of timer X mode register

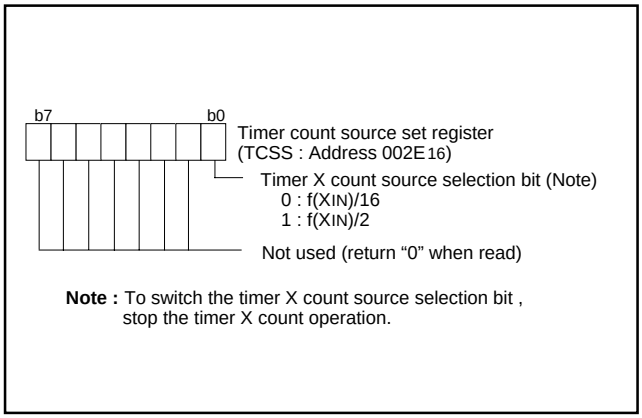


Fig. 20 Timer count source set register

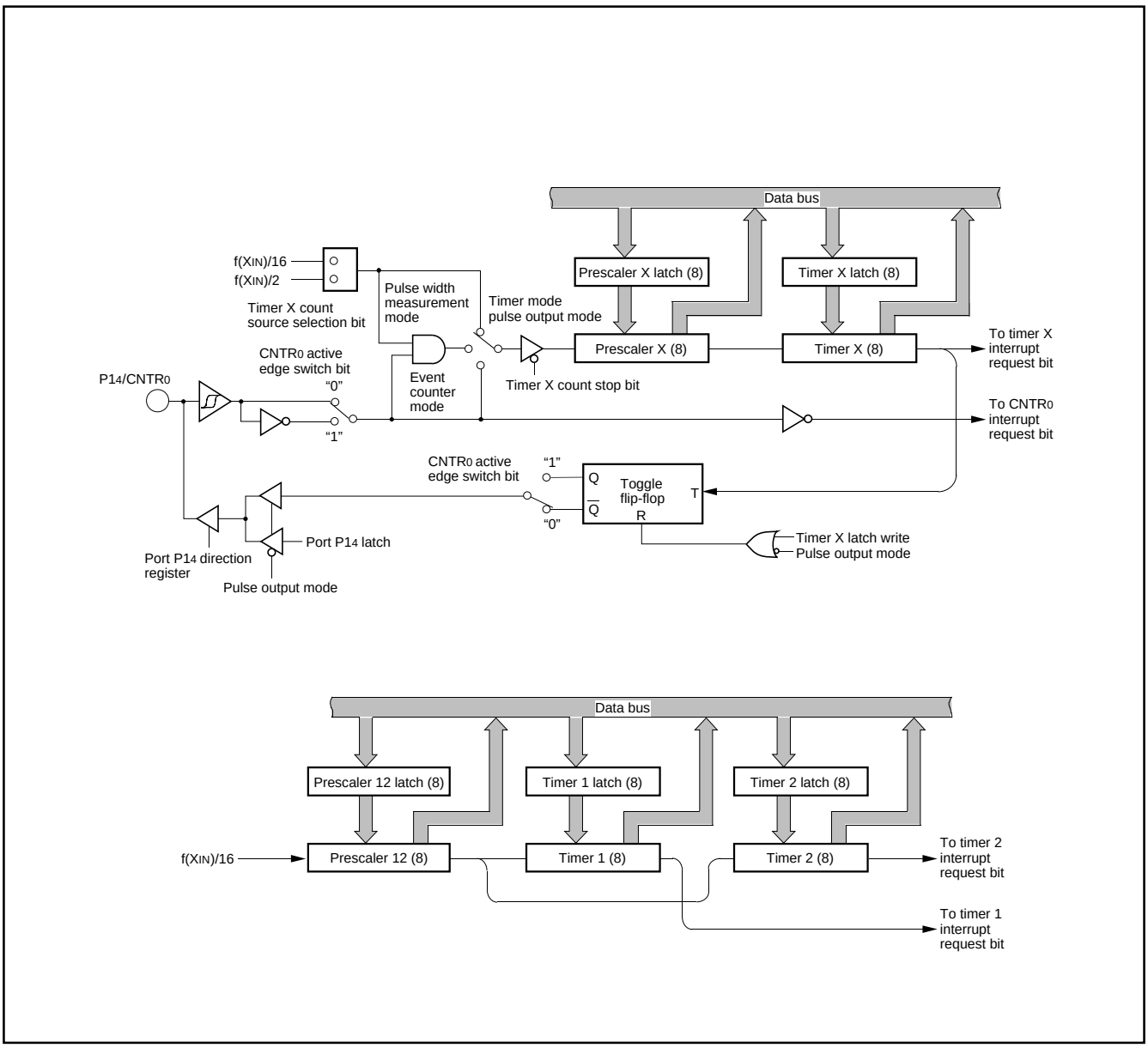


Fig. 21 Block diagram of timer X, timer 1 and timer 2

Serial Interface

●Serial I/O1

• Asynchronous serial I/O (UART) mode

Serial I/O1 can be used as an asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation when serial I/O1 is in operation.

Eight serial data transfer formats can be selected, and the transfer formats to be used by a transmitter and a receiver must be identical.

Each of the transmit and receive shift registers has a buffer register (the same address on memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the respective buffer registers. These buffer registers can also hold the next data to be transmitted and receive 2-byte receive data in succession.

By selecting "1" for continuous transmit valid bit (bit 2 of SIO1CON), continuous transmission of the same data is made possible.

This can be used as a simplified PWM.

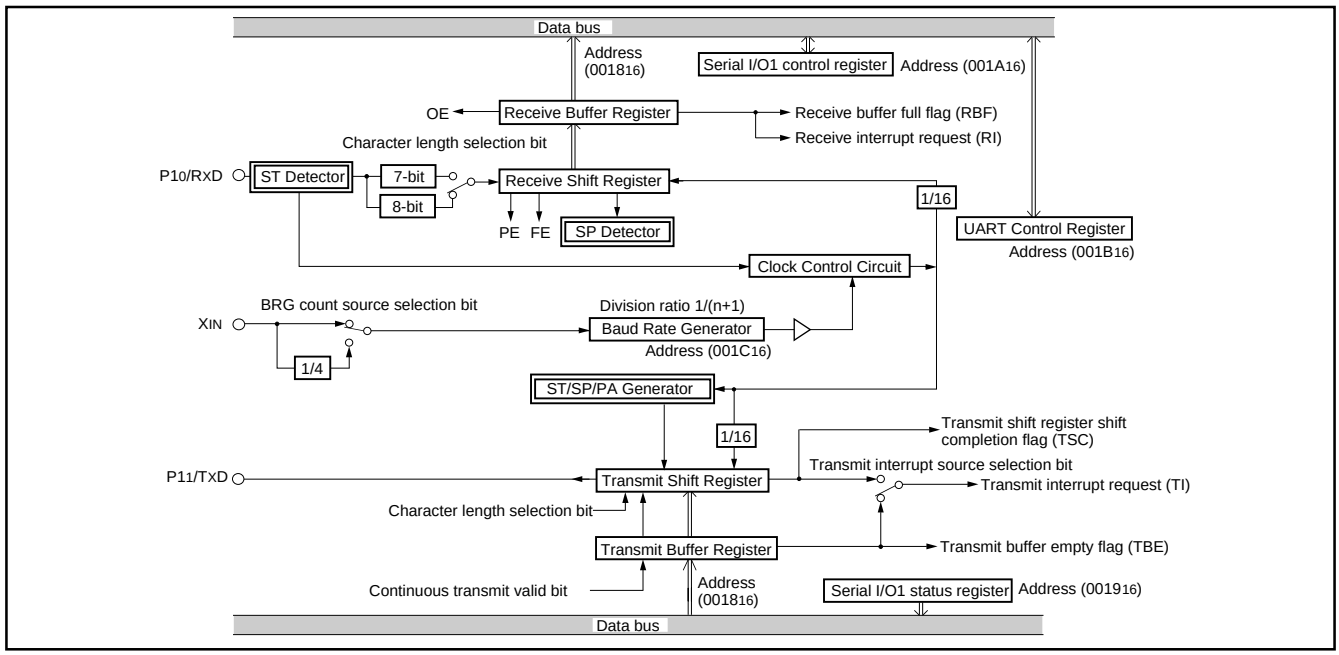
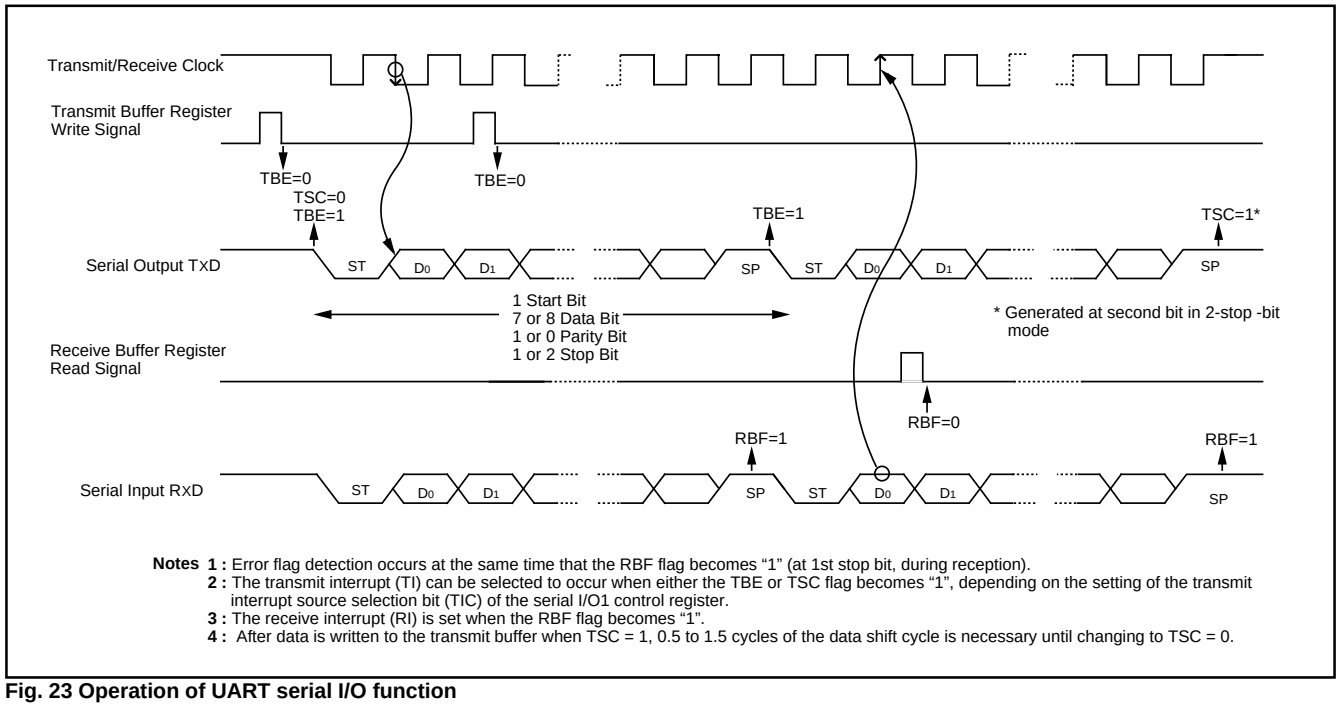


Fig. 22 Block diagram of UART serial I/O



Notes
1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes "1".
4 : After data is written to the transmit buffer when TSC = 1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC = 0.

Fig. 23 Operation of UART serial I/O function

[Serial I/O1 control register] SIO1CON

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART control register] UARTCON

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P1_1$/TxD pin.

[UART status register] UARTSTS

The read-only UART status register consists of seven flags (bits 0 to 6) which indicate the operating status of the UART function and various errors. This register functions as the UART status register (UARTSTS) when selecting the UART.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the UART status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively).

Writing “0” to the serial I/O1 mode selection bits MOD1 and MOD0 (bit 7 and 6 of the Serial I/O1 control register) also clears all the status flags, including the error flags.

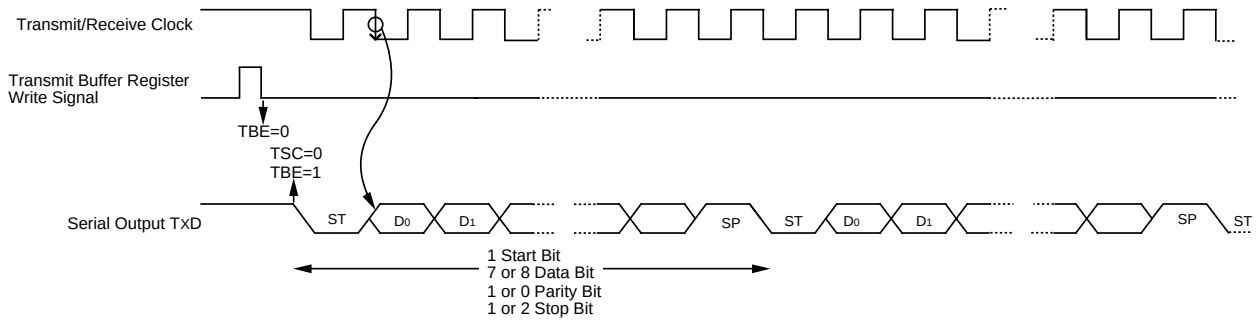
All bits of the serial I/O1 status register are initialized to “81_{16}” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the continuous transmit valid bit (bit 2) becomes “1”.

[Transmit/Receive buffer register] TB/RB

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7-bit, the MSB of data stored in the receive buffer is “0”.

[Baud Rate Generator] BRG

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.



Notes
1 : When the serial I/O1 mode selection bits (b7, b6) is “10”, the transmit enable bit is “1”, and continuous transmit valid bit is “1”, writing on the transmit buffer initiates continuous transmission of the same data.
2 : Select 0 for continuous transmit valid bit to stop continuous transmission. The TxD pin will stop at high level after completing transmission of 1 byte.
3 : If the transmit buffer contents are rewritten during a continuous transmission, transmission of the rewritten data will be started after completing transmission of 1 byte.

Fig. 24 Continuous transmission operation of UART serial I/O

• **Universal serial bus (USB) mode**

By setting bits 7 and 6 of the serial I/O1 control register (address 001A16) to "11", the USB mode is selected.

This mode conforms to Low-Speed USB2.0 specification. In this mode serial I/O1 interrupt have 6 sources; USB in and out token receive, setup token receive, USB reset, suspend, and resume. The USB status/UART status register functions as the USB status register (USBSTS).There is the USBVREFOUT pin for the USB reference voltage output, and a D-line with 1.5 kΩ external resistor can be pull up. USB mode block and USB transceiver block shown in figures 25 and 26.

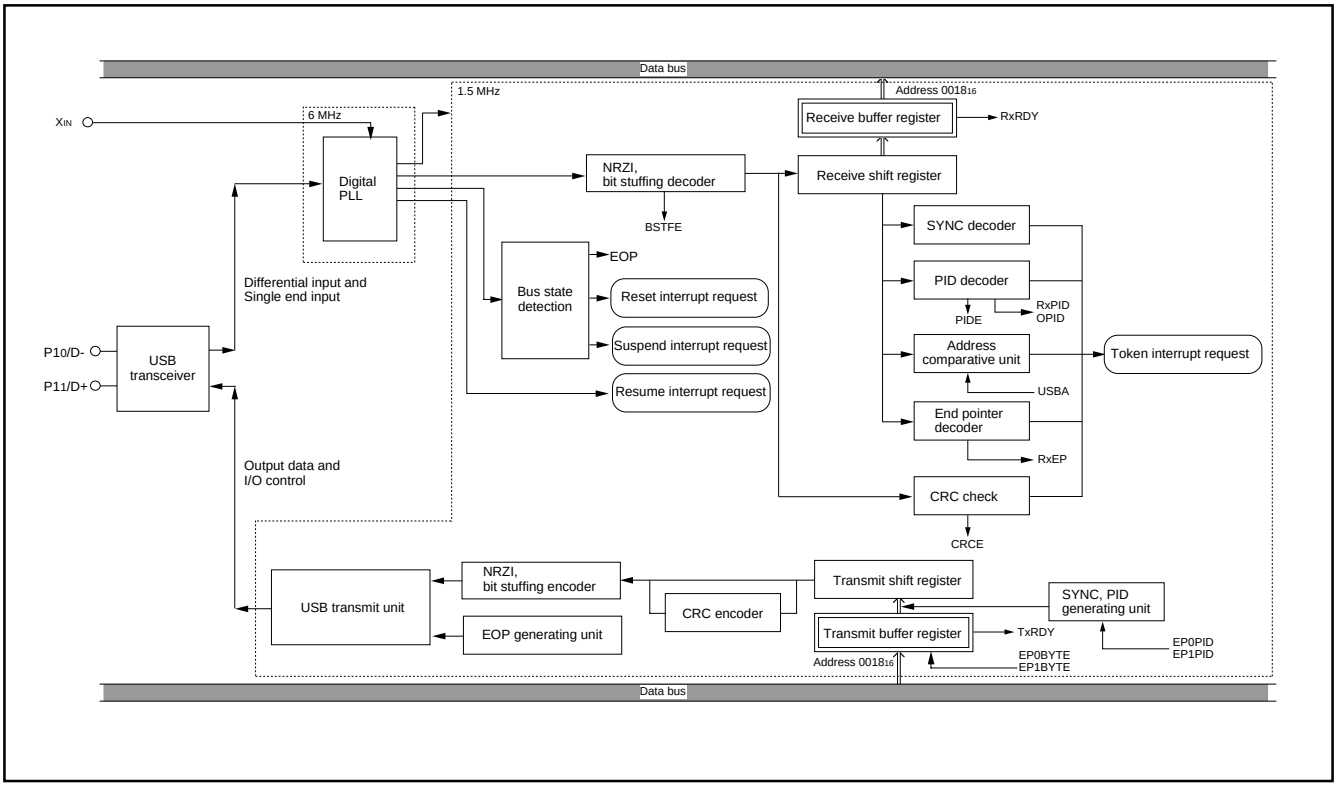


Fig. 25 USB mode block diagram

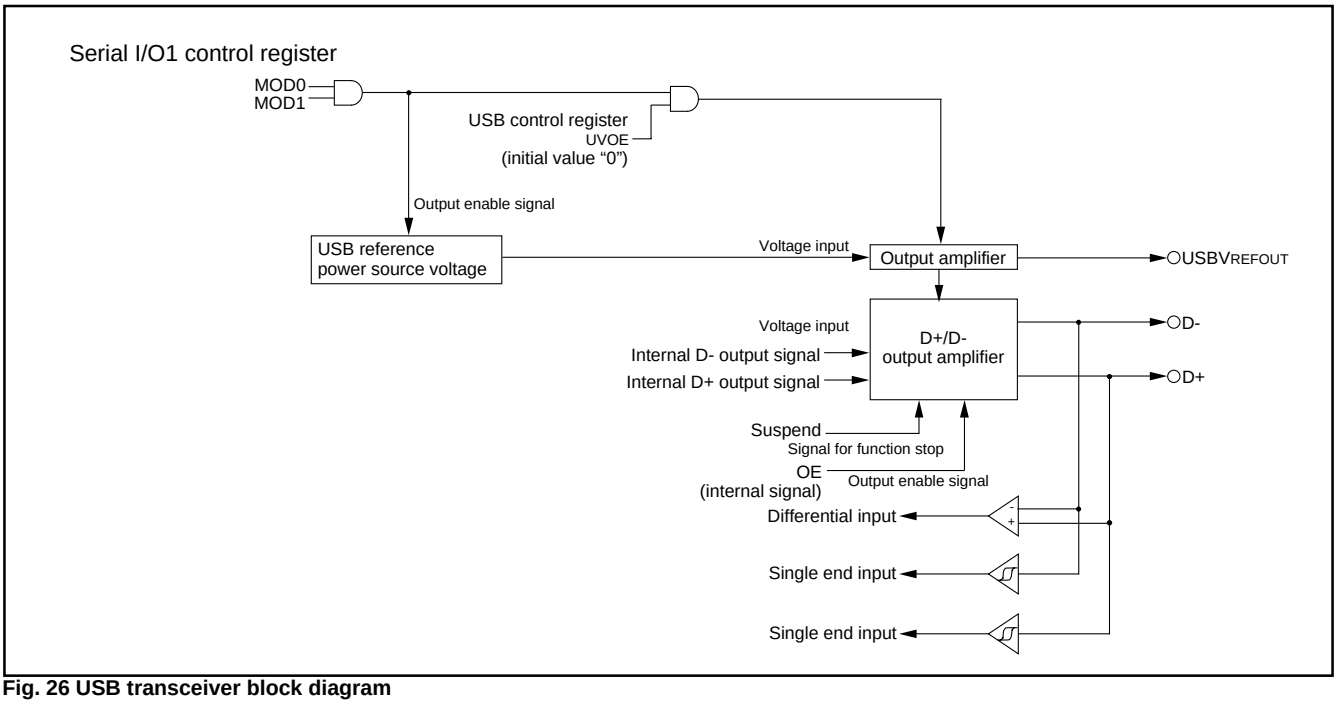


Fig. 26 USB transceiver block diagram

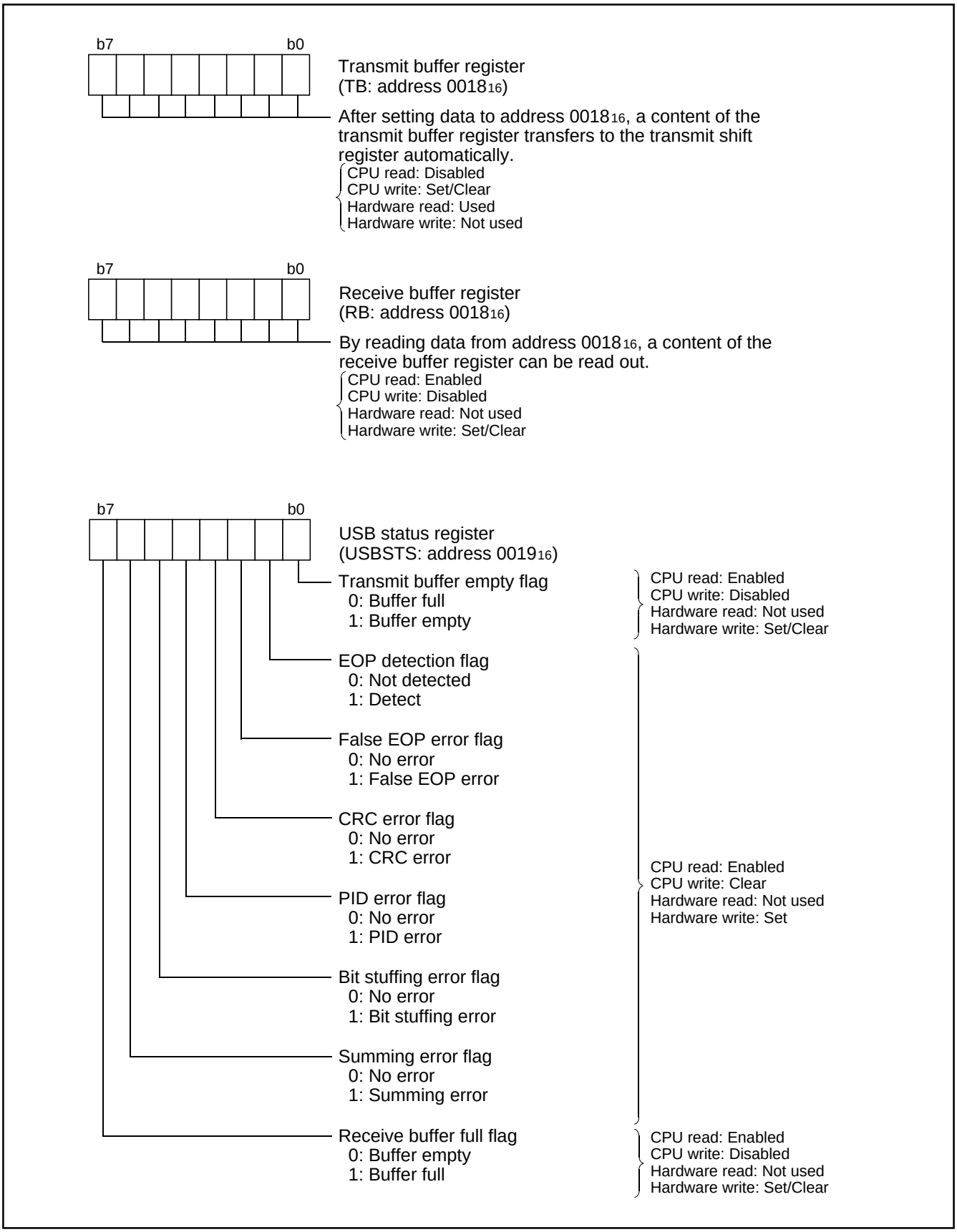


Fig. 27 Structure of serial I/O1-related registers (1)

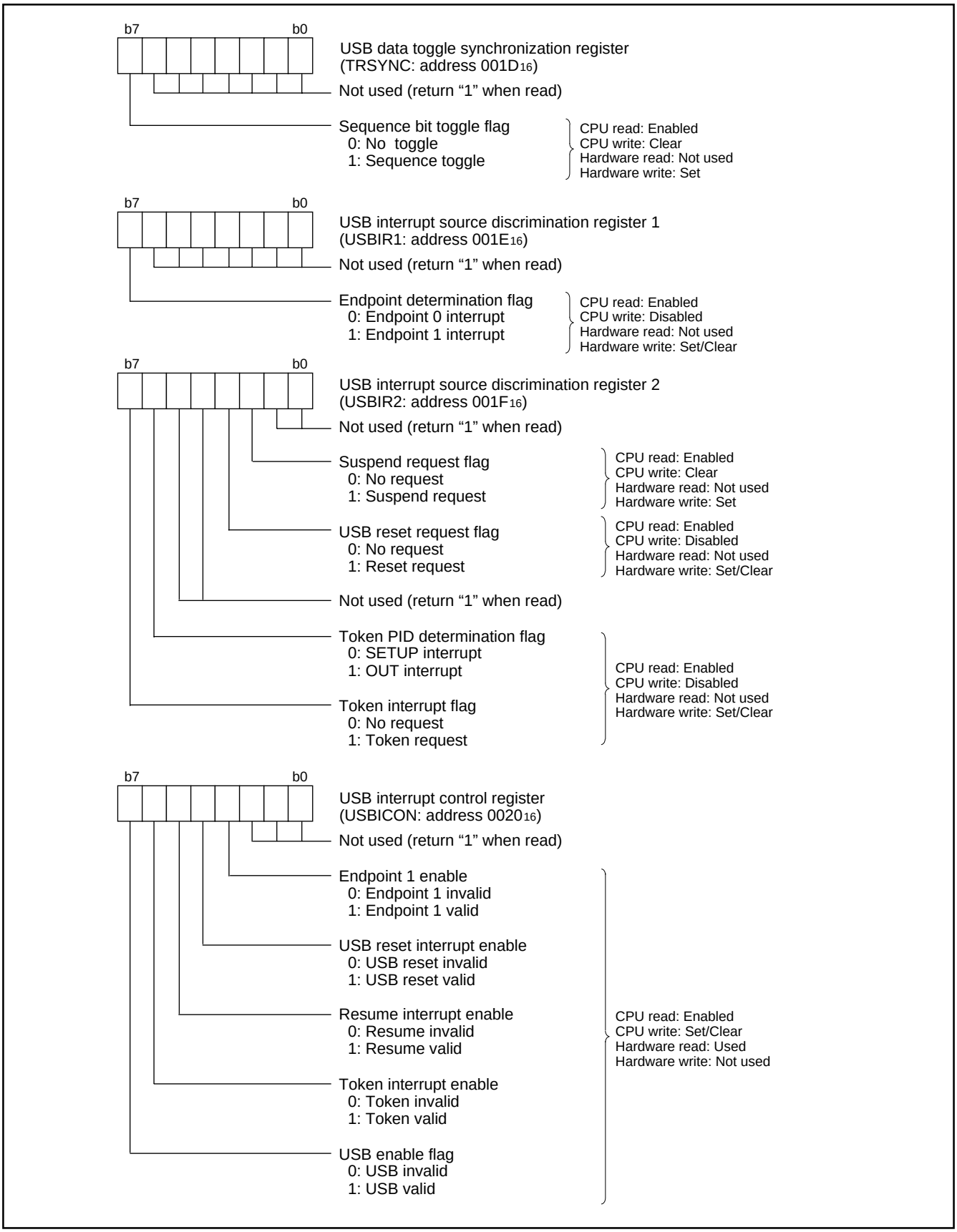


Fig. 28 Structure of serial I/O1-related registers (2)

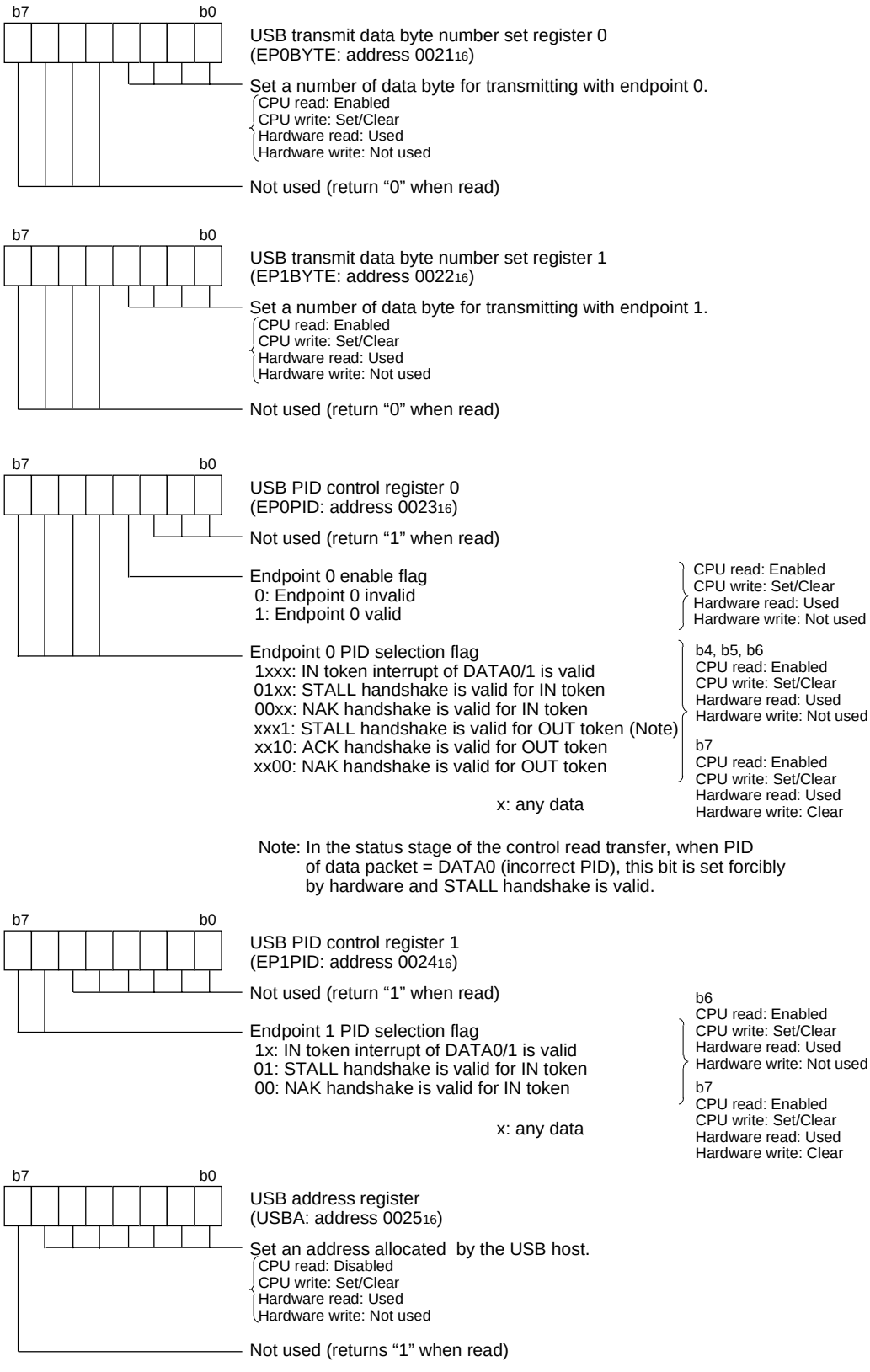


Fig. 29 Structure of serial I/O1-related registers (3)

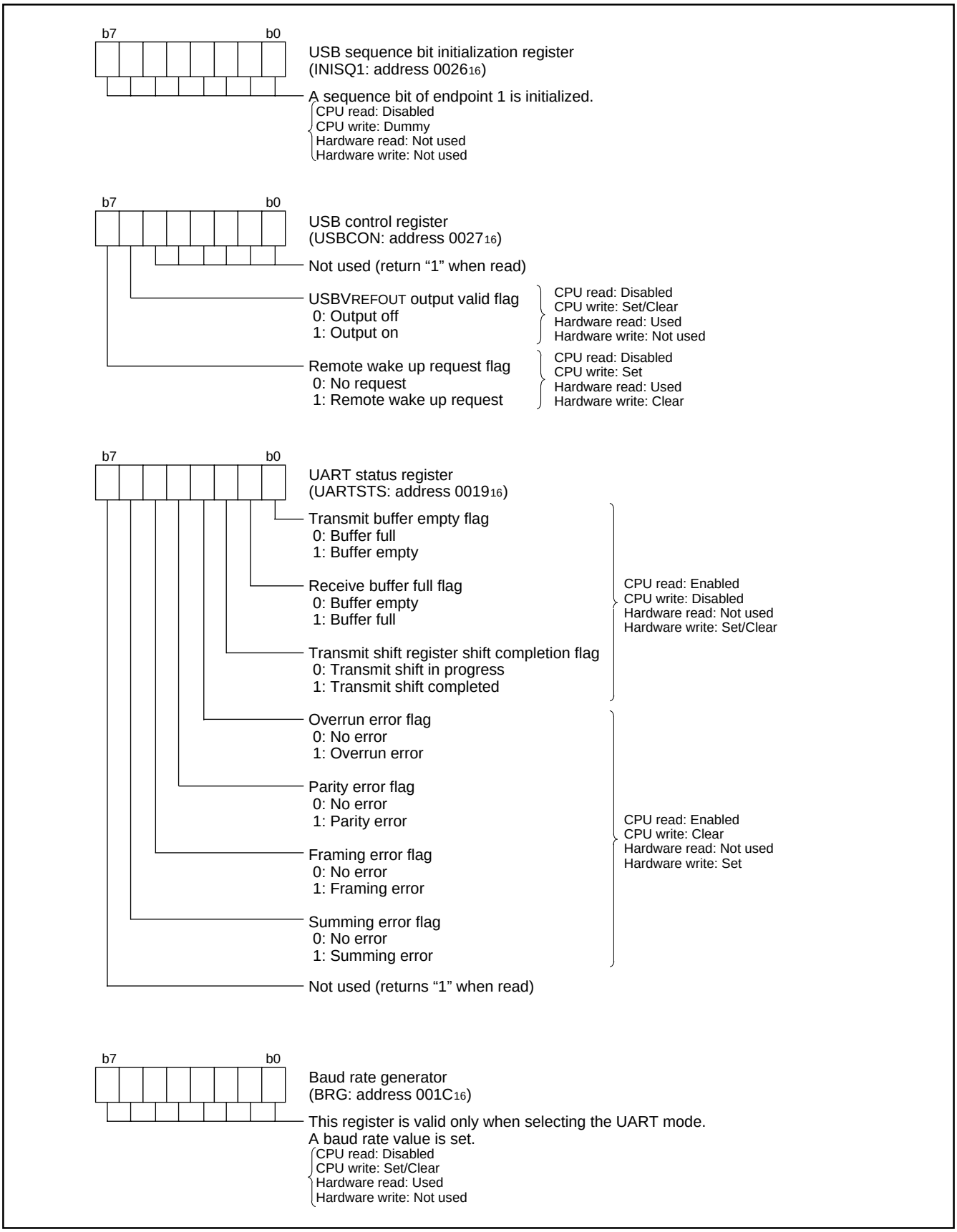


Fig. 30 Structure of serial I/O1-related registers (4)

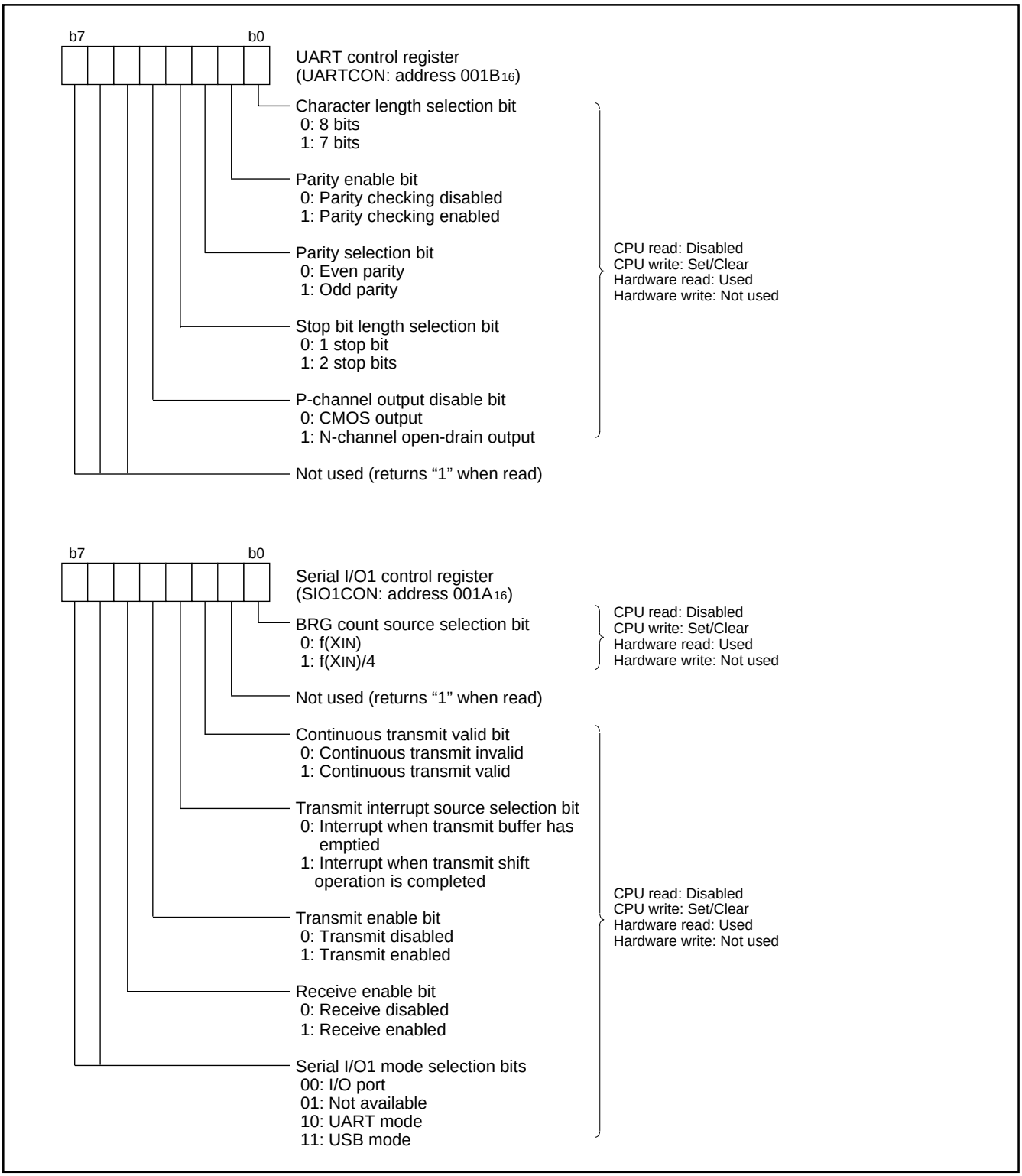


Fig. 31 Structure of serial I/O1-related registers (5)

Note on using USB mode

Handling of SE0 signal in program (at receiving)

7534 group has the border line to detect as USB RESET or EOP (End of Packet) on the width of SE0 (Single Ended 0).

A response apposite to a state of the device is expected.

The name of the following short words which is used in table 5 shows as follow.

- TKNE: Token interrupt enable (bit 6 of address 20_{16})
- RSME: Resume interrupt enable (bit 5 of address 20_{16})
- RSTE: USB reset interrupt enable (bit 4 of address 20_{16})
- Spec: A response of the device requested by Low-Speed USB2.0 specification
- SIE: Hardware operation in 7534 group
- F/W: Recommendation process in the program
- FEOPE: False EOP error flag (bit 2 of address 19_{16})
- RxPID: Token interrupt flag (bit 7 of address $1F_{16}$)

Table 5 Relation of the width of SE0 and the state of the device

		State of device				
Width of SE0		Idle state TKNE = X RSME = 0 RSTE =1	End of Token in transaction TKNE = 1 RSME = 0 RSTE =1	End of data or handshake in transaction TKNE = 0 RSME = 0 RSTE = 0 or 1	Suspend state TKNE = 0 RSME = 1 RSTE = 0	
0 µ s 0.5 µ s	Spec	Ignore	Ignore	Ignore	Spec	Reset or resume
	SIE	Keep counting suspend timer	Not detected as EOP(in case of no detection EOP, SIE returns idle state as time out. FEOPE flag is set.)	Not detected as EOP(in case of no detection EOP, SIE returns idle state as timeup. FEOPE flag is set.)		
	F/W	Not acknowledge	Not acknowledge	Wait for the next EOP flag		
0.5 µ s 2.5 µ s	Spec	Keep alive	EOP	EOP	SIE	Reset interrupt request
	SIE	Initialize suspend timer count value	Token interrupt request	Set EOP flag		
	F/W	Not acknowledge	Token interrupt processing execute	After checking the set of EOP flag, go to the next processing		
2.5 µ s 2.67 µ s	Spec	Keep alive or Reset	EOP or Reset	EOP or Reset		
	SIE	may determine as keep alive and Reset interrupt	may determine as EOP and Reset interrupt	may determine as EOP and Reset interrupt		
	F/W	Keep alive in case of no interrupt request Reset processing in case of interrupt request	RxPID = 1> Token interrupt processing RxPID = 0> Reset interrupt processing	Continue the processing in case of no interrupt request Reset processing in case of interrupt request	F/W	Reset interrupt processing Resume interrupt processing
2.67 µ s	Spec	Reset	Reset	Reset		
	SIE	Reset interrupt request	Reset interrupt request	Reset interrupt request		
	F/W	Reset processing	Reset processing	Reset processing		

• Function of USBPID control register 0 (address 0023_{16})

Bit 4 (STALL handshake control for OUT token) of this register is forcibly set by SIE under the special condition shown below.

Set condition; when PID of data packet = DATA0 (incorrect PID) in the status stage of the control read transfer.

• SYNC field at reception

Normally, the SYNC field consists of “KJKJKJKK” (8 bits). However, as for SIE of the 7534 Group, when the low-order 6 bits are “KJKJKK”, it is determined as SYNC.

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

- For receiving, set "0" to bit 3.
- When receiving, bit 7 is cleared by writing dummy data to serial I/O2 register after shift is completed.
- Bit 7 is set earlier a half cycle of shift clock than completion of shift operation. Accordingly, when checking shift completion by using this bit, the setting is as follows:
  (1) check that this bit is set to "1",
  (2) wait a half cycle of shift clock,
  (3) read/write to serial I/O2 register.

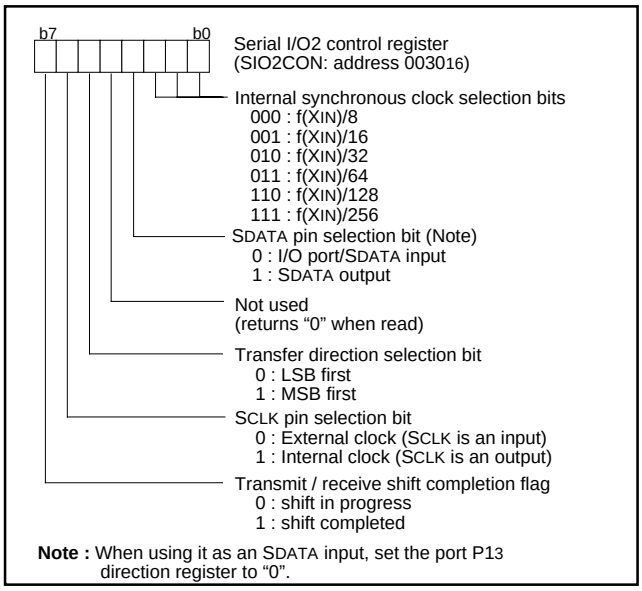


Fig. 32 Structure of serial I/O2 control registers

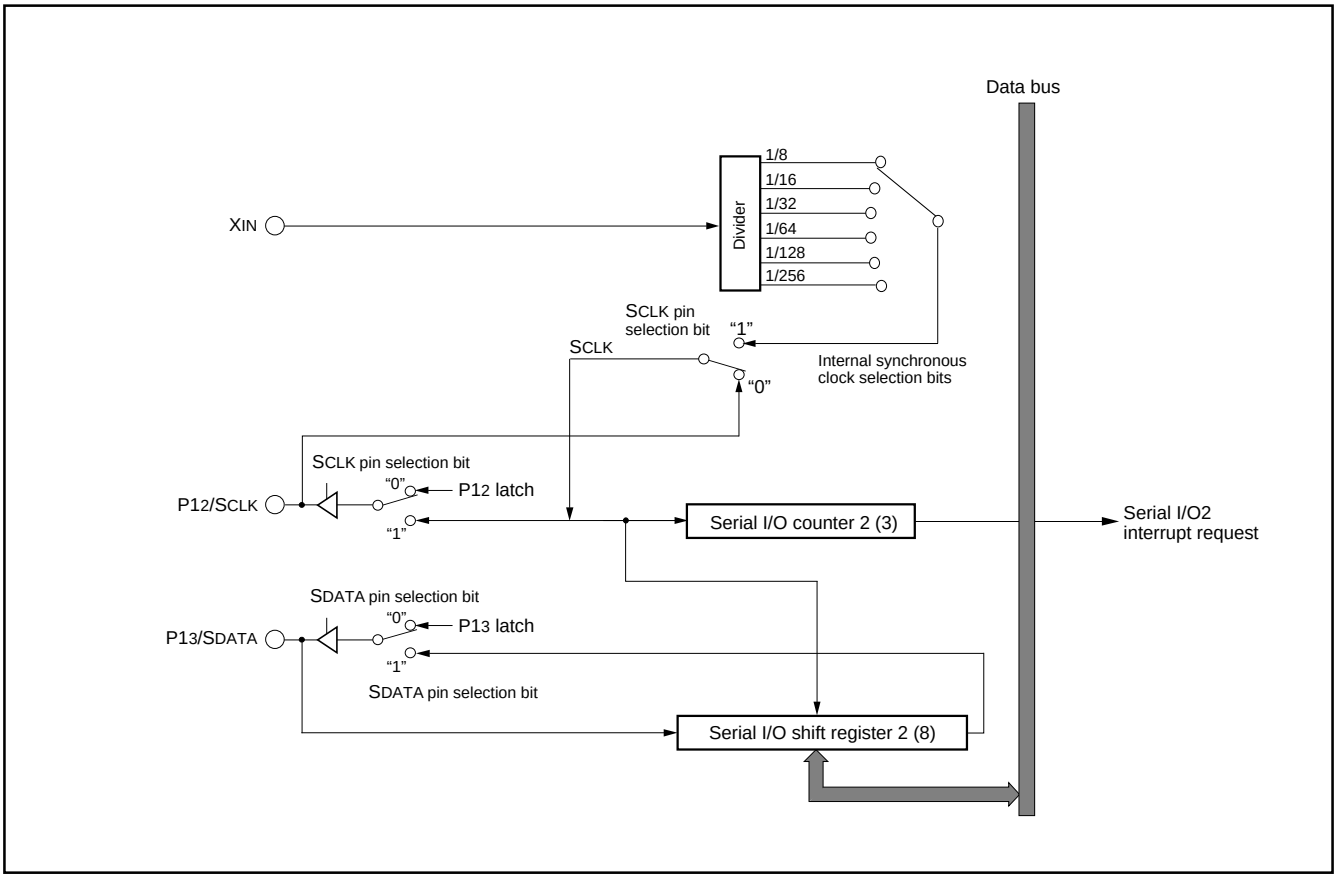


Fig. 33 Block diagram of serial I/O2

Serial I/O2 operation

By writing to the serial I/O2 register(address 0031_{16}) the serial I/O2 counter is set to “7”.

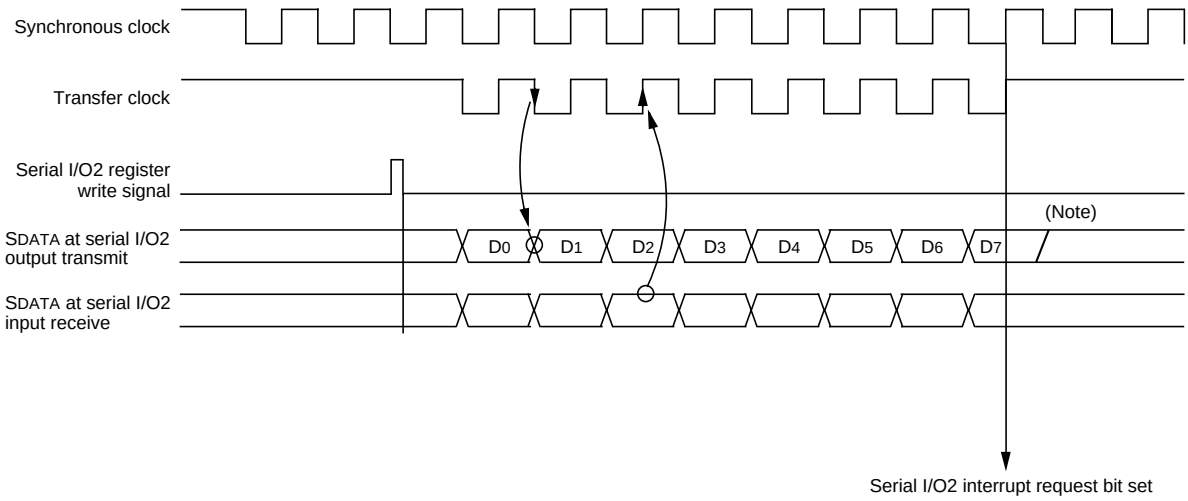
After writing, the SDATA pin outputs data every time the transfer clock shifts from a high to a low level. And, as the transfer clock shifts from a low to a high, the SDATA pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

- Serial I/O2 counter is cleared to “0”.
- Transfer clock stops at an “H” level.
- Interrupt request bit is set.
- Shift completion flag is set.

Also, the SDATA pin is in a high impedance state after the data transfer is complete. Refer to Figure 34.

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA pin is not in a high impedance state on the completion of data transfer.



Note : When the internal clock is selected as the transfer and the direction register of P1 3/SDATA pin is set to the input mode, the SDATA pin is in a high impedance state after the data transfer is completed.

Fig. 34 Serial I/O2 timing (LSB first)

A/D Converter

The functional blocks of the A/D converter are described below.

[A/D conversion register] AD

The A/D conversion register is a read-only register that stores the result of A/D conversion. Do not read out this register during an A/D conversion.

[A/D control register] ADCON

The A/D control register controls the A/D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at “0” during A/D conversion, and changes to “1” at completion of A/D conversion.
A/D conversion is started by setting this bit to “0”.

[Comparison voltage generator]

The comparison voltage generator divides the voltage between V_{SS} and V_{REF} by 1024 by a resistor ladder, and outputs the divided voltages. Since the generator is disconnected from V_{REF} pin and V_{SS} pin, current is not flowing into the resistor ladder.

[Channel Selector]

The channel selector selects one of ports $P2_7/AN_7$ to $P2_0/AN_0$, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A/D conversion register. When A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”. Because the comparator is constructed linked to a capacitor, set f(X_{IN}) to 500 kHz or more during A/D conversion.

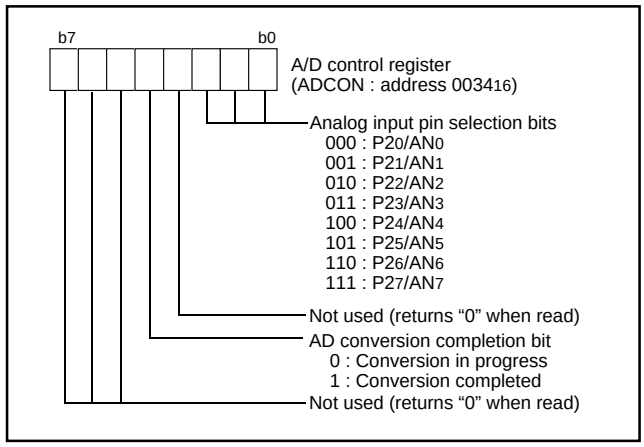


Fig. 35 Structure of A/D control register

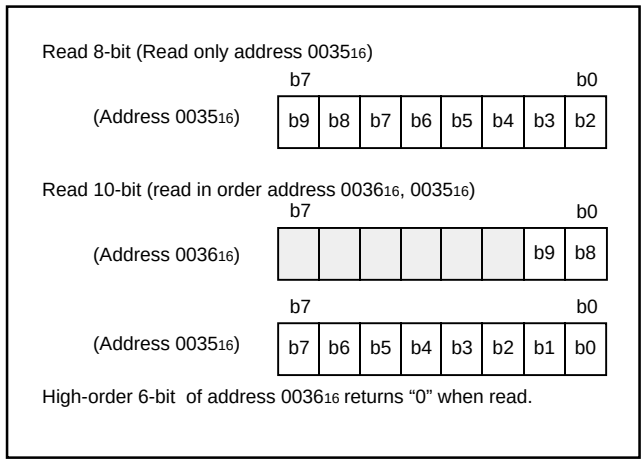


Fig. 36 Structure of A/D conversion register

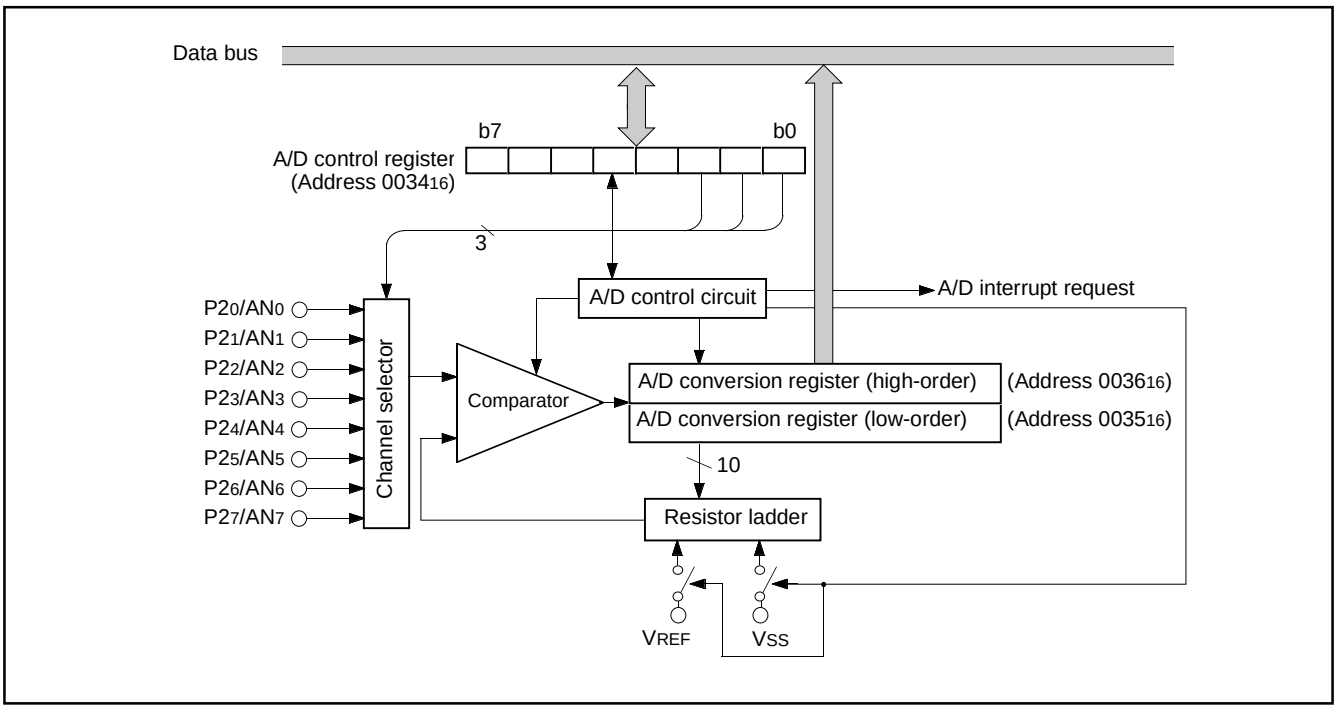


Fig. 37 Block diagram of A/D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.

When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 174.763 ms at f(XIN)=6 MHz.

When this bit is "1", the count source becomes f(XIN)/16. In this case, the detection time is 683 µs at f(XIN)=6 MHz.

This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.

Once this bit is set to "1", it cannot be changed to "0" by program.

This bit is cleared to "0" after reset.

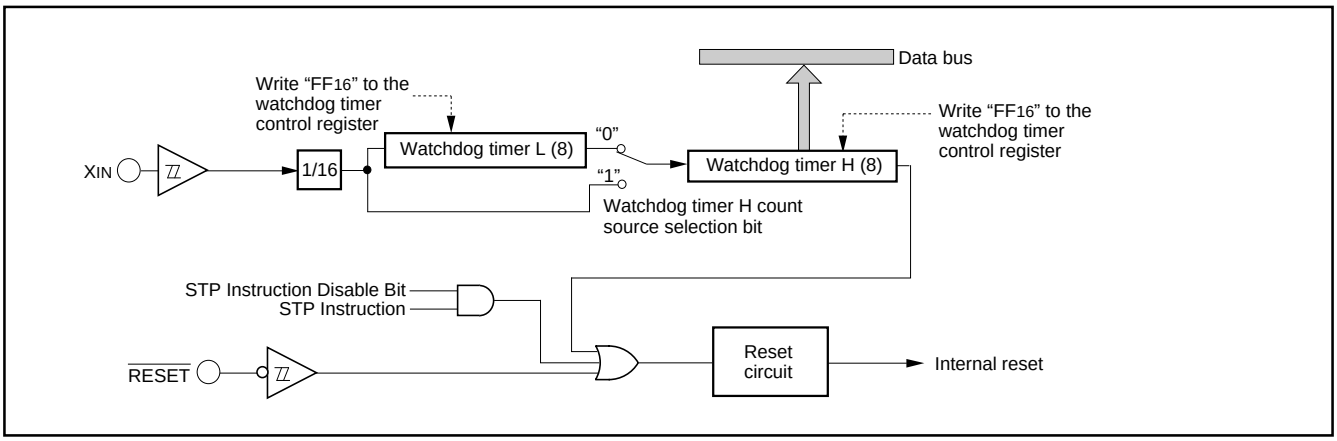


Fig. 38 Block diagram of watchdog timer

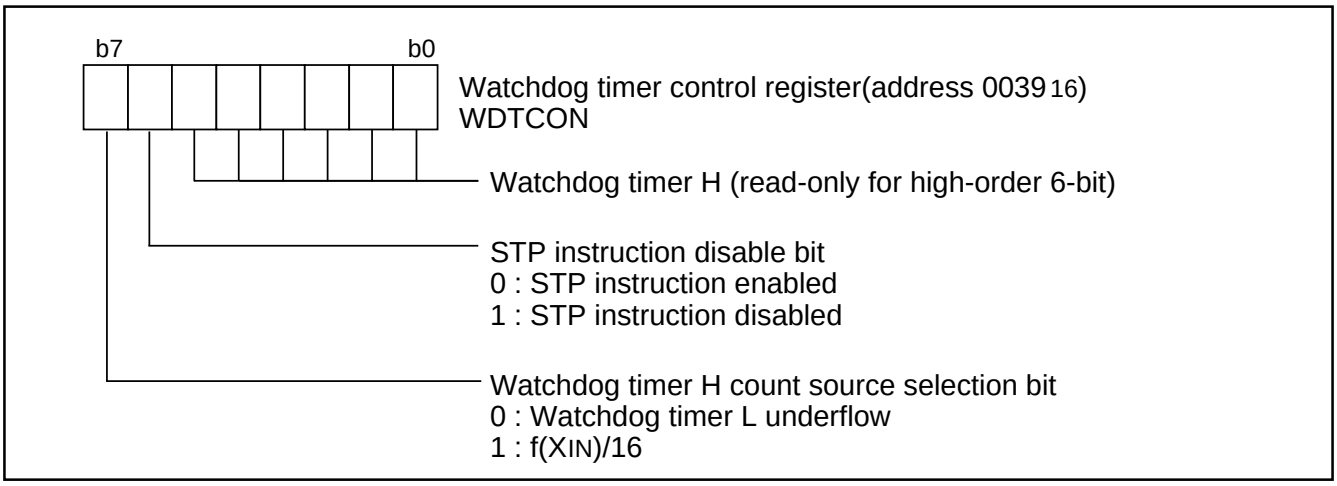


Fig. 39 Structure of watchdog timer control register

Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{\text{RESET}}$ pin at the “L” level for 15 µs or more when the power source voltage is 4.1 to 5.5 V and X_{IN} is in stable oscillation.

After that, this reset status is released by returning the $\overline{\text{RESET}}$ pin to the “H” level. The program starts from the address having the contents of address $FFFD_{16}$ as high-order address and the contents of address $FFFC_{16}$ as low-order address.

Note that the reset input voltage should be 0.82 V or less when the power source voltage passes 4.1 V.

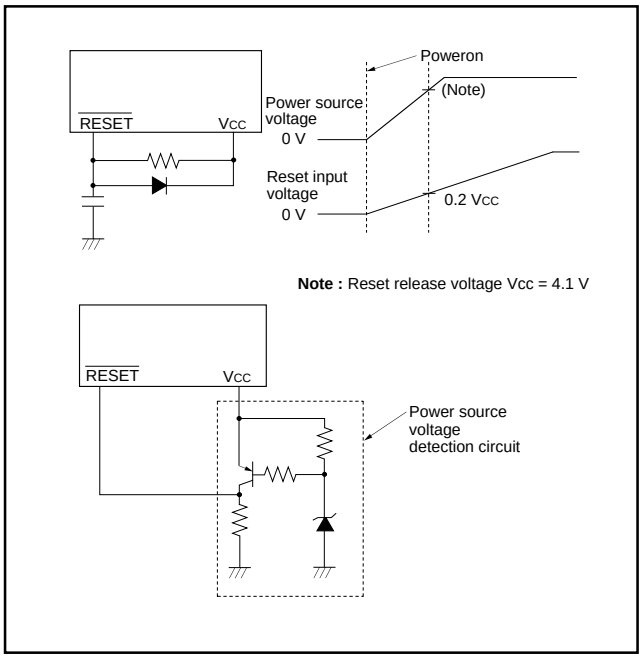


Fig. 40 Example of reset circuit

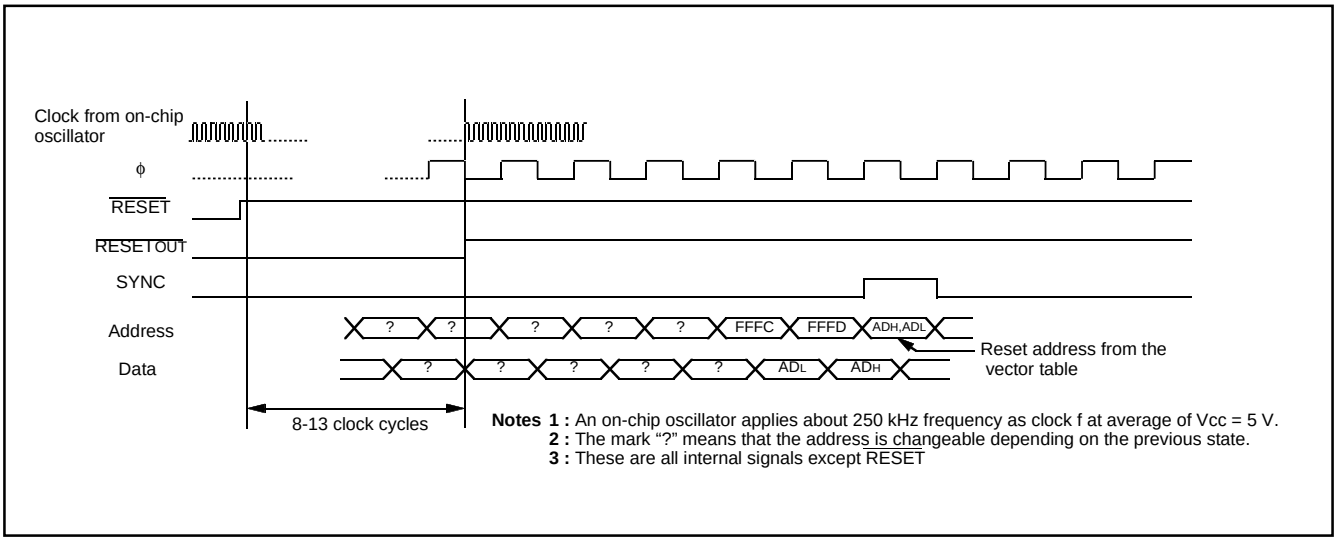


Fig. 41 Timing diagram at reset

	Address	Register contents
(1) Port P0 direction register	0001_{16}	00_{16}
(2) Port P1 direction register	0003_{16}	X 0 0 0 0 0 0 0
(3) Port P2 direction register	0005_{16}	00_{16}
(4) Port P3 direction register	0007_{16}	00_{16}
(5) Port P4 direction register	0009_{16}	X X X X X X 0 0
(6) Pull-up control register	0016_{16}	FF_{16}
(7) USB/UART status register	0019_{16}	1 0 0 0 0 0 0 1
(8) Serial I/O1 control register	$001A_{16}$	02_{16}
(9) UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(10) USB data toggle synchronization register	$001D_{16}$	0 1 1 1 1 1 1 1
(11) USB interrupt source discrimination register 1	$001E_{16}$	0 1 1 1 1 1 1 1
(12) USB interrupt source discrimination register 2	$001F_{16}$	0 1 1 1 0 0 1 1
(13) USB interrupt control register	0020_{16}	0 0 0 0 0 1 1 1
(14) USB transmit data byte number set register 0	0021_{16}	00_{16}
(15) USB transmit data byte number set register 1	0022_{16}	00_{16}
(16) USBPID control register 0	0023_{16}	0 0 0 0 0 1 1 1
(17) USBPID control register 1	0024_{16}	0 0 1 1 1 1 1 1
(18) USB address register	0025_{16}	1 0 0 0 0 0 0 0
(19) USB sequence bit initialization register	0026_{16}	1 1 1 1 1 1 1 1
(20) USB control register	0027_{16}	0 0 1 1 1 1 1 1
(21) Prescaler 12	0028_{16}	FF_{16}
(22) Timer 1	0029_{16}	01_{16}
(23) Timer 2	$002A_{16}$	00_{16}
(24) Timer X mode register	$002B_{16}$	00_{16}
(25) Prescaler X	$002C_{16}$	FF_{16}
(26) Timer X	$002D_{16}$	FF_{16}
(27) Timer count source set register	$002E_{16}$	00_{16}
(28) Serial I/O2 control register	0030_{16}	00_{16}
(29) A/D control register	0034_{16}	10_{16}
(30) MISRG	0038_{16}	00_{16}
(31) Watchdog timer control register	0039_{16}	0 0 1 1 1 1 1 1
(32) Interrupt edge selection register	$003A_{16}$	00_{16}
(33) CPU mode register	$003B_{16}$	1 0 0 0 0 0 0 0
(34) Interrupt request register 1	$003C_{16}$	00_{16}
(35) Interrupt control register 1	$003E_{16}$	00_{16}
(36) Processor status register	(PS)	X X X X X 1 X X
(37) Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$

Note X : Undefined

Fig. 42 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT.

Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

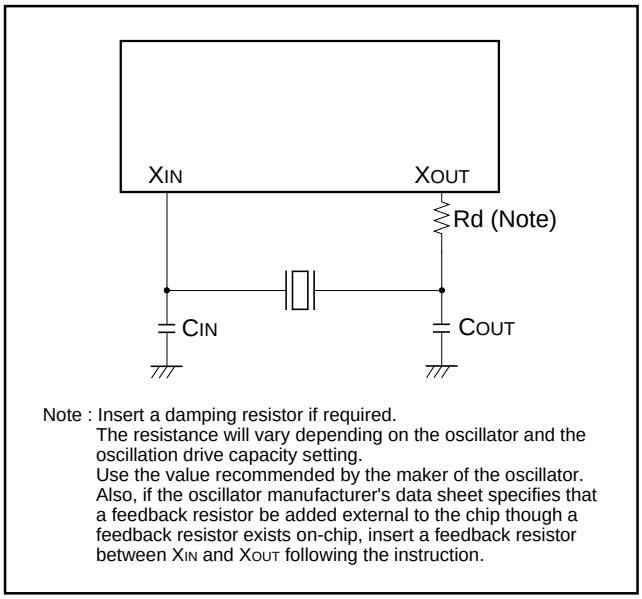


Fig. 43 External circuit of ceramic resonator

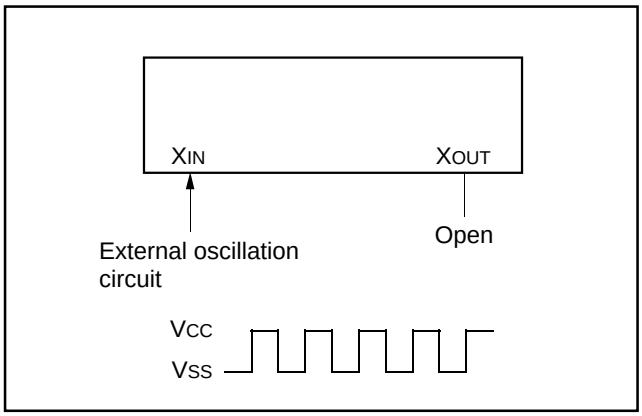


Fig. 44 External clock input circuit

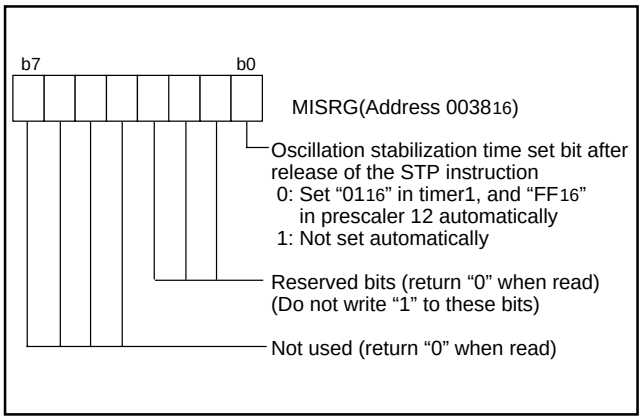


Fig. 45 Structure of MISRG

●Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock ϕ stops at an “H” level and the XIN oscillator stops. At this time, timer 1 is set to “0116” and prescaler 12 is set to “FF16” when the oscillation stabilization time set bit after release of the STP instruction is “0”.

On the other hand, timer 1 and prescaler 12 are not set when the above bit is “1”. Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used.

f(XIN)/16 is forcibly connected to the input of prescaler 12.

When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at “H” until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation.

In case oscillation is restarted by reset, no wait time is generated. So apply an “L” level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an “H” level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.

Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to “1” before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting clock which is XIN divided by 16, so set the timer 1 interrupt enable bit to “0” before the STP instruction is executed.

Note

For use with the oscillation stabilization set bit after release of the STP instruction set to “1”, set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Clock mode

Operation is started by an on-chip oscillator after releasing reset.

A division ratio (1/1,1/2,1/8) is selected by setting bits 7 and 6 of the CPU mode register after releasing it.

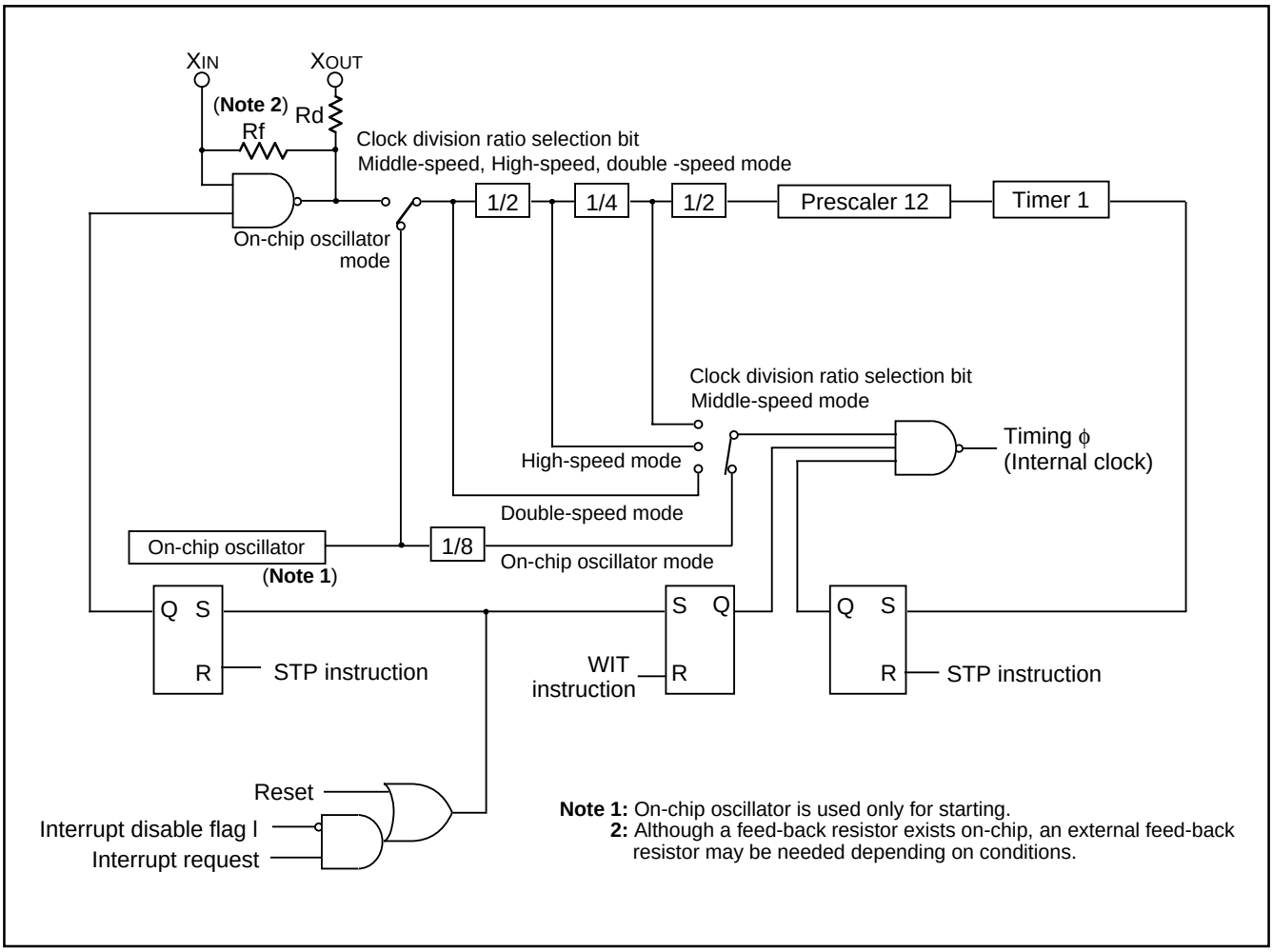


Fig. 46 Block diagram of system clock generating circuit (for ceramic resonator)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is “1”. After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to “1”, then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When a count source of timer X is switched, stop a count of timer X.

Ports

- The values of the port direction registers cannot be read.
  That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is “1”, addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
  It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
  For setting direction registers, use the LDM instruction, STA instruction, etc.
- As for the 36-pin version, set "1" to each bit 6 of the port P3 direction register and the port P3 register.
- As for the 32-pin version, set “1” to respective bits 5, 6, 7 of the port P3 direction register and port P3 register.

A/D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(X_{IN}) is 500kHz or more during A/D conversion.
Do not execute the STP instruction during A/D conversion.

Watchdog Timer

The internal reset may not be generated correctly in the middle-speed mode, depending on the underflow timing of the watchdog timer.
When using the watchdog timer, operate the MCU in any mode other than the middle-speed mode (i.e., high-speed, low-speed or double-speed mode).

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock f is the same as that of the XIN in double-speed mode, twice the XIN cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

Note on Stack Page

When 1 page is used as stack area by the stack page selection bit, the area which can be used as stack depends on RAM size. Especially, be careful that the RAM area varies in Mask ROM version, One Time PROM version and Emulator MCU.

NOTES ON USE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, an electrolytic or a ceramic capacitor of 1.0 µF is recommended.

Handling of USBV_{REFOUT} Pin

In order to prevent the instability of the USBV_{REFOUT} output due to external noise, connect a capacitor as bypass capacitor between USBV_{REFOUT} pin and GND pin (V_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor, a ceramic or electrolytic capacitor of 0.22 µF is recommended.

USB Communication

- In applications requiring high-reliability, we recommend providing the system with protective measures such as USB function initialization by software or USB reset by the host to prevent USB communication from being terminated unexpectedly, for example due to external causes such as noise.
- When USB suspend mode with TTL level on $P1_0$, $P1_2$, $P1_3$ input level selection bit (bit 3 of address 17_{16}) set to “1”, suspend current as I_{CC} might be greater than 300 µA as a spec.
  [Countermeasure]
  There are two countermeasures by software to avoid it as follows.
  (1) Change from TTL input level to CMOS input level for $P1_0$, $P1_2$, $P1_3$ port input.
  (2) Change from TTL input level to CMOS input level before STP instruction in suspend routine;
  then after RESUME or Remote wake up interrupt, return to TTL input level from CMOS input level. That is shown in Figure 47.

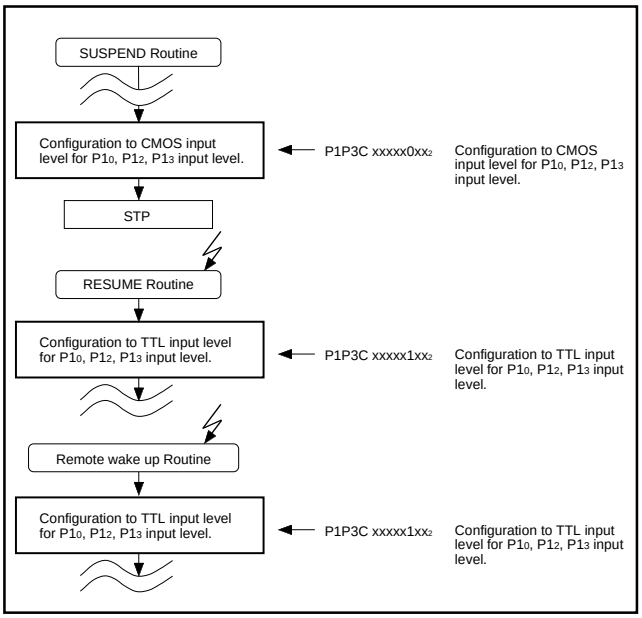


Fig. 47 Countermeasure (2) by software

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

Electric Characteristic Differences Among Mask ROM and One TIme PROM Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation among mask ROM and One Time PROM version MCUs due to the differences in the manufacturing processes.

When manufacturing an application system with One Time PROM version and then switching to use of the mask ROM version, perform sufficient evaluations for the commercial samples of the mask ROM version.

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Note on A/D Converter

Method to stabilize A/D Converter is described below.

(a) A/D conversion accuracy could be affected for Bus Powered*1 USB devices, while the communicating.
Figure 48 shows the method to stabilize A/D conversion accuracy, inserting a capacitor between Vref and V_{SS}.
*1: Power supplied by USB V_{CC} BUS.

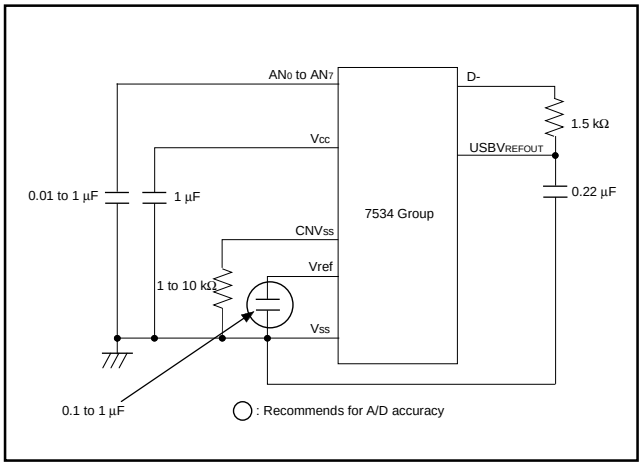


Fig. 48 Method to stabilize A/D conversion accuracy

(b) It is recommended for A/D accuracy to avoid converting while USB communication, and use average value of several converted values.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form
..... (three identical copies) or one floppy disk

* For the mask ROM confirmation and the mark specifications, refer to the “Renesas Technology Corp.” Homepage (http://www.renesas.com).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 6 Special programming adapter

Package	Name of Programming Adapter
PLQP0032GB-A	PCA7435GPG03
PRSP0036GA-A	PCA7435FP, PCA7435FPG02
PRDP0042BA-A	PCA7435SP, PCA7435SPG02

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 49 is recommended to verify programming.

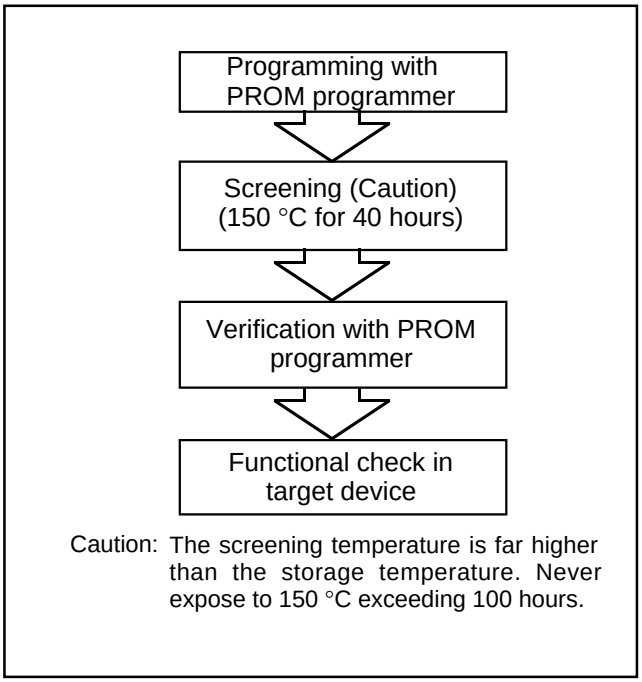


Fig. 49 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 7 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}, $P4_0$, $P4_1$		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}, $USBV_{REFOUT}$, $P4_0$, $P4_1$		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	(Note 2)	Ta = 25°C	1000 (Note 3)	mW
T_{opr}	Operating temperature			–20 to 85	°C
T_{stg}	Storage temperature			–40 to 125	°C

Notes 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for mask ROM version.
2: The rating value depends on packages.
3: This is the value for 42-pin version.
The value of the 36-pin version is 300 mW.
The value of the 32-pin version is 200 mW.

Recommended Operating Conditions

Table 8 Recommended operating conditions
(V_{CC} = 4.1 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X_{IN}) = 6 MHz	4.1	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$	0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$	2.0		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}	0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	D+, D-	2.0		3.6	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$	0		0.3 V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$	0		0.8	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	D+, D-	0		0.8	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$I_{OH(peak)}$	“H” total peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$			–80	mA
$I_{OL(peak)}$	“L” total peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_7$, $P4_0$, $P4_1$			80	mA
$I_{OL(peak)}$	“L” total peak output current (Note 1)	$P3_0$–$P3_6$			60	mA
$I_{OH(avg)}$	“H” total average output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$			–40	mA
$I_{OL(avg)}$	“L” total average output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_7$, $P4_0$, $P4_1$			40	mA
$I_{OL(avg)}$	“L” total average output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(peak)}$	“H” peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$			–10	mA
$I_{OL(peak)}$	“L” peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_7$, $P4_0$, $P4_1$			10	mA
$I_{OL(peak)}$	“L” peak output current (Note 2)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	“H” average output current (Note 3)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$			–5	mA
$I_{OL(avg)}$	“L” average output current (Note 3)	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_7$, $P4_0$, $P4_1$			5	mA
$I_{OL(avg)}$	“L” average output current (Note 3)	$P3_0$–$P3_6$			15	mA
f(X_{IN})	Oscillation frequency (Note 4) at ceramic oscillation or external clock input	V_{CC} = 4.1 to 5.5 V Double-speed mode			6	MHz

Note 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics

Table 9 Electrical characteristics (1) (V_{CC} = 4.1 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.1 to 5.5 V	V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 4.1 to 5.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage	D+, D-	V_{CC} = 4.4 to 5.25 V Pull-down through 15kΩ ±5 % for D+, D- Pull-up through 1.5kΩ ±5 % by $USBV_{REFOUT}$ for D- (Ta = 0 to 70 °C)	2.8		3.6	V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_7$, $P4_0$, $P4_1$	I_{OL} = 5 mA V_{CC} = 4.1 to 5.5 V			1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.1 to 5.5 V			0.3	V
V_{OL}	"L" output voltage	D+, D-	V_{CC} = 4.4 to 5.25 V Pull-down through 15kΩ ±5 % for D+, D- Pull-up through 1.5kΩ ±5 % by $USBV_{REFOUT}$ for D-(Ta = 0 to 70 °C)			0.3	V
V_{OL}	"L" output voltage	$P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.1 to 5.5 V			2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.1 to 5.5 V			0.3	V
V_{T+}–V_{T-}	Hysteresis	D+, D-			0.15		V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, INT_0, INT_1 (Note 2), $P0_0$–$P0_7$(Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis	RxD, SCLK, SDATA (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$	V_I = V_{CC} (Pin floating. Pull-up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_6$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$	V_I = V_{SS} (Pin floating. Pull-up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull-up transistors"on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V

Note 1: $P1_1$ is measured when the P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: RxD, SCLK, SDATA, INT_0 and INT_1 have hystereses only when bits 0, 1 and 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake-up.

Table 10 Electrical characteristics (2)
(Vcc = 4.1 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
ICC	Power source current	Double-speed mode, f(XIN) = 6 MHz, Output transistors “off”			6	10	mA
		f(XIN) = 6 MHz, (in WIT state) Output transistors “off”			1.6	3.2	mA
		Increment when A/D conversion is executed f(XIN) = 6 MHz, VCC = 5 V			0.8		mA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA
		VCC = 4.4 V to 5.25 V Oscillation stopped in USB mode USB (SUSPEND), (pull-up resistor output included) (Fig. 48)	Ta = 0 to 70 °C			300	µA

A/D Converter Characteristics

Table 11 A/D Converter characteristics (1) (Vcc = 4.1 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	VCC = 4.1 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	VCC = 4.1 to 5.5 V Ta = 25 °C			±0.9	LSB
VOT	Zero transition voltage	VCC = VREF = 5.12 V	0	5	20	mV
VFST	Full scale transition voltage	VCC = VREF = 5.12 V	5105	5115	5125	mV
tCONV	Conversion time				122	tc(XIN)
RLADDER	Ladder resistor			55		kΩ
IVREF	Reference power source input current	VREF = 5.0 V	50	150	200	µA
		VREF = 3.0 V	30	70	120	
II(AD)	A/D port input current				5.0	µA

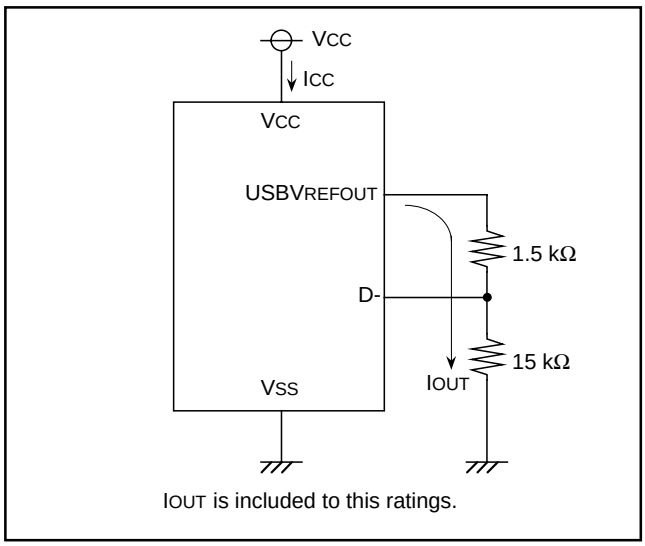


Fig. 50 Power source current measurement circuit in USB mode at oscillation stop

Timing Requirements

Table 12 Timing requirements (Vcc = 4.1 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tW(RESET)	Reset input “L” pulse width	15			µs
tC(XIN)	External clock input cycle time	166			ns
tWH(XIN)	External clock input “H” pulse width	70			ns
tWL(XIN)	External clock input “L” pulse width	70			ns
tC(CNTR)	CNTR0 input cycle time	200			ns
tWH(CNTR)	CNTR0, INT0, INT1 input “H” pulse width	80			ns
tWL(CNTR)	CNTR0, INT0, INT1 input “L” pulse width	80			ns
tC(SCLK)	Serial I/O2 clock input cycle time	1000			ns
tWH(SCLK)	Serial I/O2 clock input “H” pulse width	400			ns
tWL(SCLK)	Serial I/O2 clock input “L” pulse width	400			ns
tsu(SDATA–SCLK)	Serial I/O2 input set up time	200			ns
th(SCLK–SDATA)	Serial I/O2 input hold time	200			ns

Switching Characteristics

Table 13 Switching characteristics (Vcc = 4.1 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWH(SCLK)	Serial I/O2 clock output “H” pulse width	tC(SCLK)/2–30			ns
tWL(SCLK)	Serial I/O2 clock output “L” pulse width	tC(SCLK)/2–30			ns
td(SCLK–SDATA)	Serial I/O2 output delay time			140	ns
tv(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
tr(SCLK)	Serial I/O2 clock output rising time			30	ns
tf(SCLK)	Serial I/O2 clock output falling time			30	ns
tr(CMOS)	CMOS output rising time (Note)		10	30	ns
tf(CMOS)	CMOS output falling time (Note)		10	30	ns
tr(D+), tr(D-)	USB output rising time, CL = 200 to 450 pF, Ta = 0 to 70 °C, VCC = 4.4 to 5.25 V	75	150	300	ns
tf(D+), tf(D-)	USB output falling time, CL = 200 to 450 pF, Ta = 0 to 70 °C, VCC = 4.4 to 5.25 V	75	150	300	ns

Notes: XOUT pin is excluded.

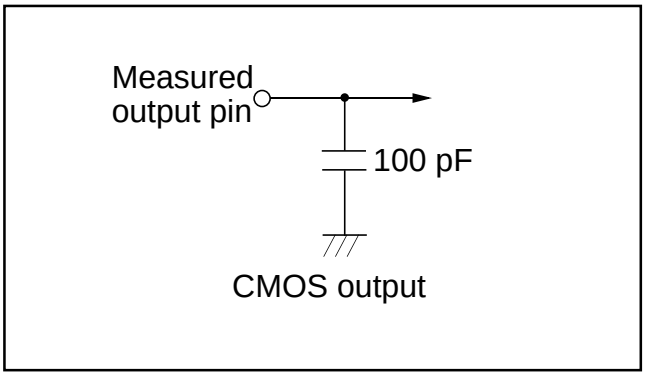


Fig. 51 Output switching characteristics measurement circuit

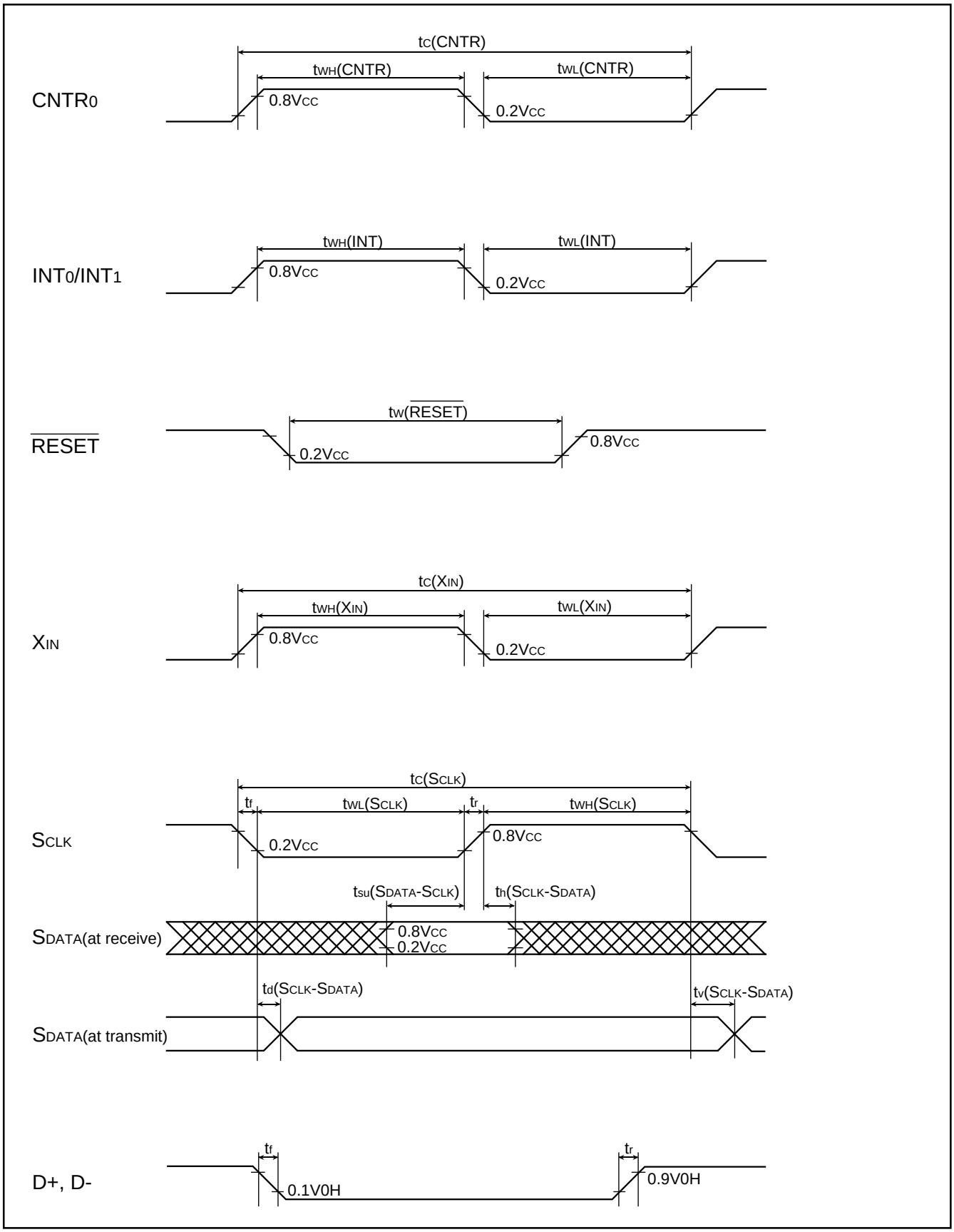


Fig. 52 Timing chart

Description of improved USB function for 7534 Group

Table 14 Description of improved USB function for 7534 Group

No.	Parameter	7532/7536 Group	7534 Group
1	Response at Control transfer	Not deal with the host which performs the Control transfer in parallel to plural device.	Connectable to the host which performs the Control transfer in parallel to plural device.
2	D+/D- transceiver circuit	USB function can be used only at the condition of C_L = 150 pF to 350 pF.	Deal with the the following USB Spefification Rev. 1.1. C_L = 200 pF to 450 pF, Trise and Tfall: 75 ns to 300 ns, Tr/Tf: 80 % to 125 %, Cross over Voltage: 1.3 V to 2.0 V.
3	Power dissipation at Suspend	Rating is Max. 300 µA not including the output current of USBV_{REFOUT}.	Rating is Max. 300 µA including the output current of USBV_{REFOUT}, by low-power dissipation of D+/D- input circuit and 3.3 V-regulator.
4	STALL in Status stage	ACK is returned once to OUT (DATA0) to be valid in Status stage.	STALL is set automaticcally by hardware when OUT (DATA0) is received in Status stage.
5	6-bit decode of SYNC field	SYNC is detected only when 8-bit full code (80_{16}) is complete.	SYNC is detected only the low-order 6 bits even if the high-order 2 bits are corrupted.

Differences among 32-pin, 36-pin and 42-pin

The 7534 Group has three package types, and each of the number of I/O ports are different. Accordingly, when the pins which have the function except a port function are eliminated, be careful that the functions are also eliminated.

Table 15 Differences among 32-pin, 36-pin and 42-pin

I/O port	42-pin SDIP	36-pin SSOP	32-pin LQFP
Port P1	$P1_0$–$P1_6$ (7-bit structure)	$P1_0$–$P1_4$ (5-bit structure)	$P1_0$–$P1_4$ (5-bit structure)
Port P2	$P2_0$–$P2_7$ (8-bit structure) (A/D converter 8-channel)	$P2_0$–$P2_7$ (8-bit structure) (A/D converter 8-channel)	$P2_0$–$P2_5$ (6-bit structure) (A/D converter 6-channel)
Port P3	$P3_0$–$P3_7$ (8-bit structure) (INT_0, INT_1 available)	$P3_0$–$P3_5$, $P3_7$ (7-bit structure) (INT_0 available)	$P3_0$–$P3_4$ (5-bit structure) (INT function not available)
Port P4	$P4_0$, $P4_1$ (2-bit structure)	No port	No port

Additionally, there are differences of SFR usage and functional definitions.

Table 16 Differences among 32-pin, 36-pin and 42-pin (SFR)

Register (Address)	42-pin SDIP	36-pin SSOP	32-pin LQFP
Port P1/Direction (02_{16}/03_{16})	Bit 7 not available	Bits 5 to 7 not available	Bits 5 to 7 not available
Port P2/Direction (04_{16}/05_{16})	All bits available	All bits available	Bits 6 and 7 not available
Port P3/Direction (06_{16}/07_{16})	All bits available	Bit 6 not available	Bits 5 to 7 not available
Port P4/Direction (08_{16}/09_{16})	Bits 2 to 7 not available	All bits not available	All bits not available
Pull-up control (16_{16})	Bit 6 definition: "$P3_5$, $P3_6$ pull-up control" Bit 7 definition: "$P3_7$ pull-up control"	Bit 6 definition: "$P3_5$ pull-up control" Bit 7 definition: "$P3_7$ pull-up control"	Bits 6 and 7 not available
Port P1P3 control (17_{16})	Bit 0 definition: "$P3_7$/INT_0 input level selection" Bit 1 definition: "$P3_6$/INT_1 input level selection"	Bit 0 definition: "$P3_7$/INT_0 input level selection" Bit 1 not available	Bits 0 and 1 not available
A/DControl (34_{16})	Bits 0 to 2 "Input pins selected by setting these bits to 000 to 111"	Bits 0 to 2 "Input pins selected by setting these bits to 000 to 111"	Bits 0 to 2 "Input pins selected by setting these bits to 000 to 101"
Interrupt edge selection ($3A_{16}$)	Bit 0 definition "INT_0 interrupt edge selection" Bit 1 definition "INT_1 interrupt edge selection" Bit 4 definition "Serial I/O1, INT_1 interrupt selection"	Bit 0 definition "INT_0 interrupt edge selection" Bits 1 and 4 not available	Bits 0, 1 and 4 not available
Interrupt request ($3C_{16}$)	Bit 1 definition "UART transmission, USB (except IN), INT_1" Bit 2 definition "INT_0"	Bit 1 definition "UART transmission, USB (except IN)" Bit 2 definition "INT_0"	Bit 1 definition "UART transmission, USB (except IN)" Bit 2 not available
Interrupt control ($3E_{16}$)	Bit 1 definition "UART transmission, USB (except IN), INT_1" Bit 2 definition "INT_0"	Bit 1 definition "UART transmission, USB (except IN)" Bit 2 definition "INT_0"	Bit 1 definition "UART transmission, USB (except IN)" Bit 2 not available

Description supplement for use of USB function stably

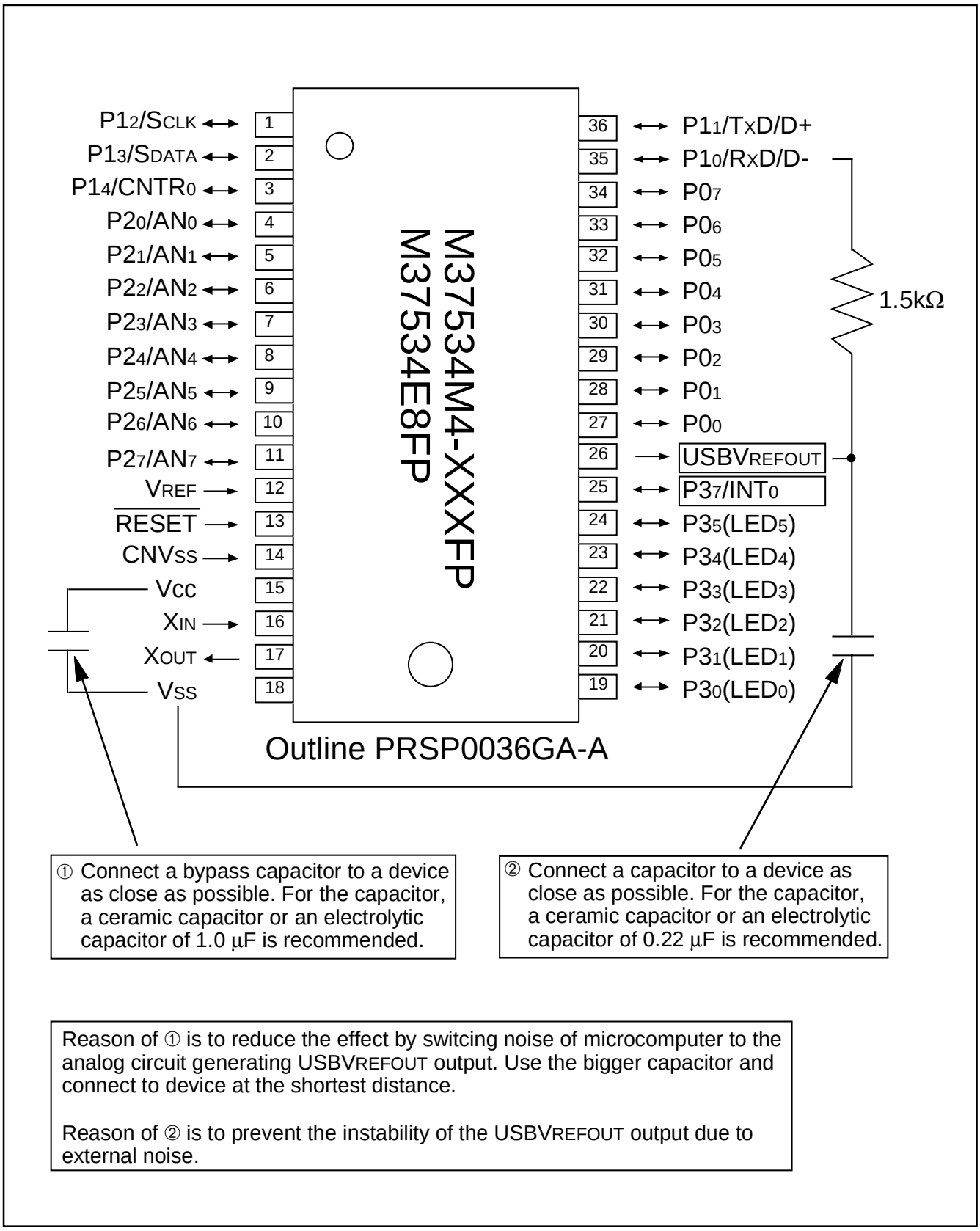


Fig. 53 Handling of VCC, USBVREFOUT pins of M37534M4-XXXFP, M37534E8FP

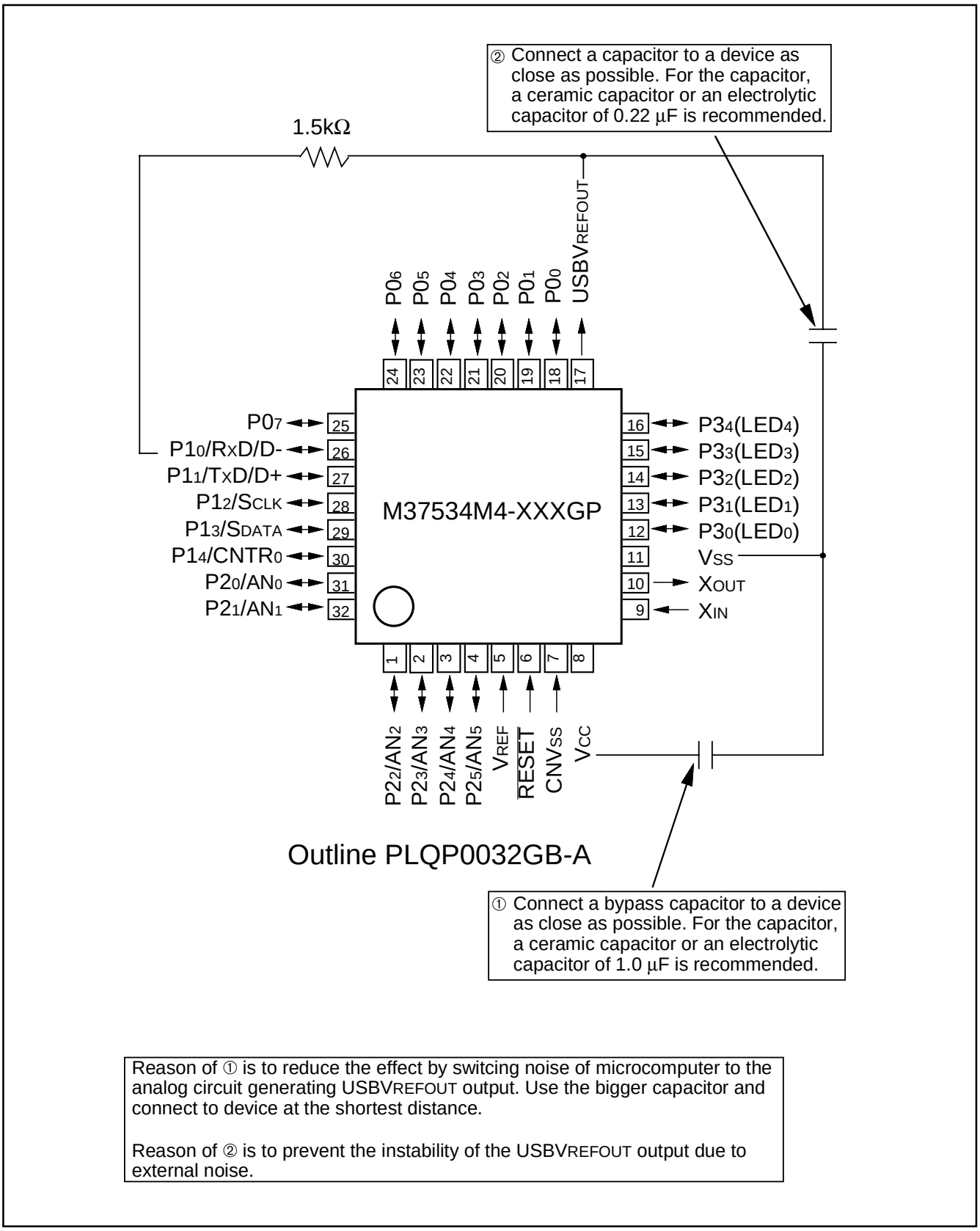


Fig. 54 Handling of VCC, USBVREFOUT pins of M37534M4-XXXGP

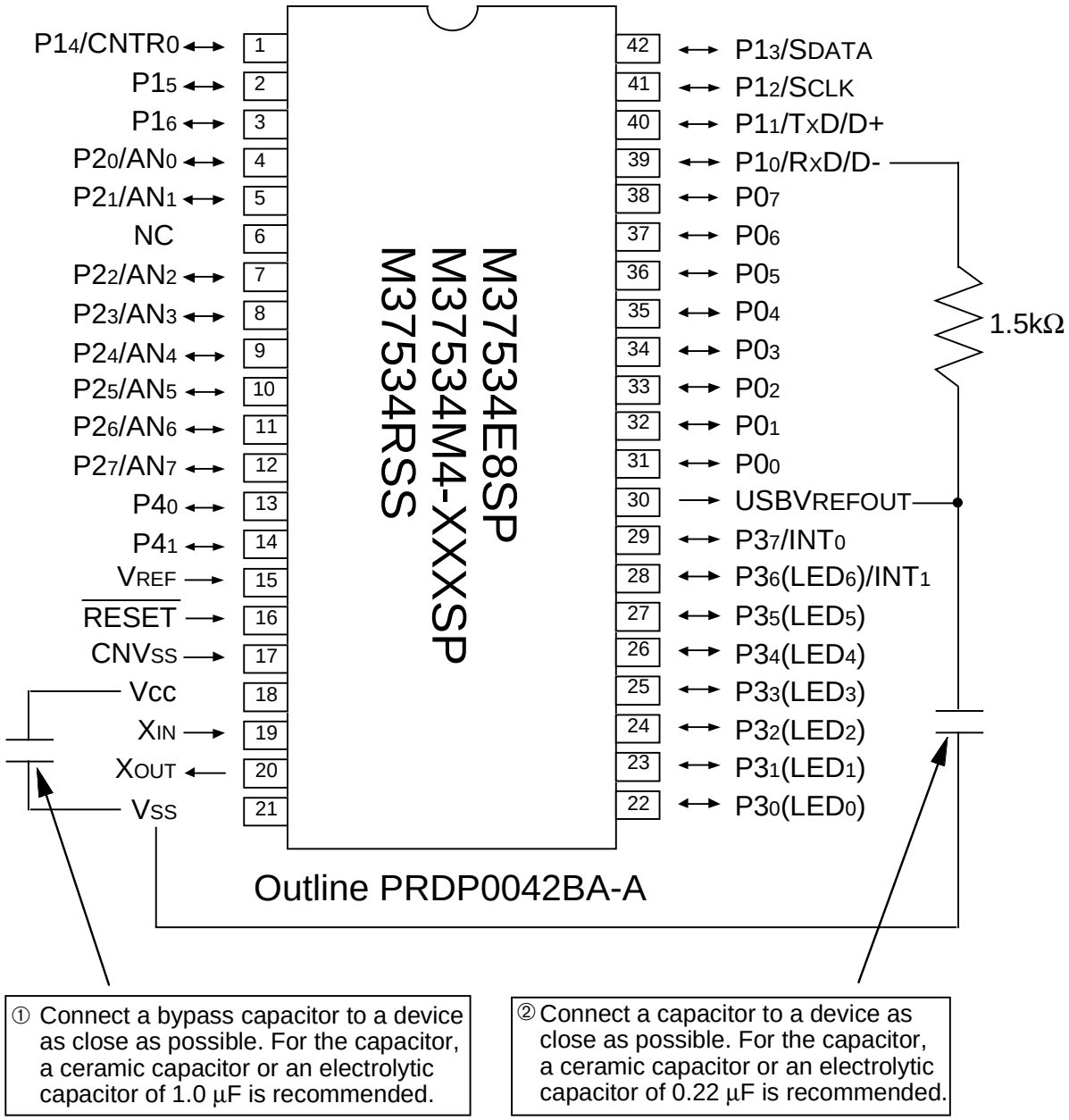
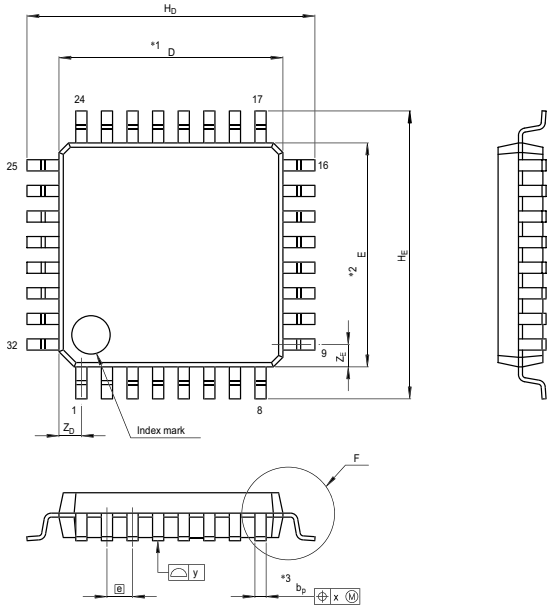


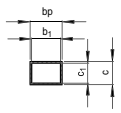
Fig. 55 Handling of Vcc, USBVREFOUT pins of M37534E8SP, M37534M4-XXXSP, M37534RSS

PACKAGE OUTLINE

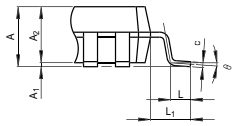
PLQP0032GB-A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g





Terminal cross section



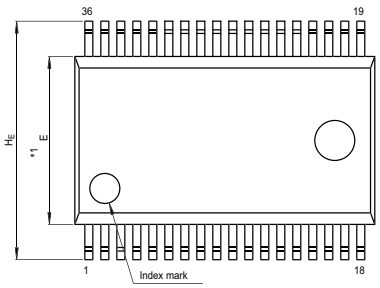
Detail F

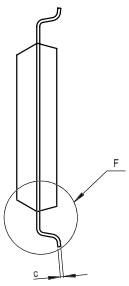
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

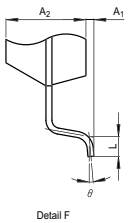
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

PRSP0036GA-A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-A	36P2R-A	0.5g







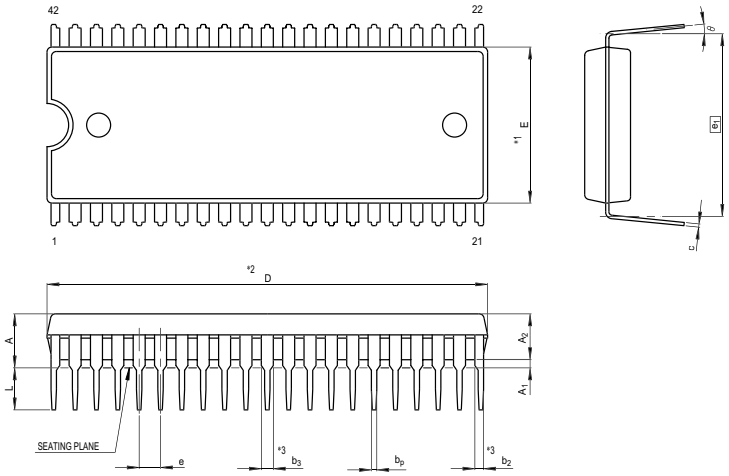
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A_2	—	2.0	—
A	—	—	2.4
A_1	0.05	—	—
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

PRDP0042BA-A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP42-13x36.72-1.78	PRDP0042BA-A	42P4B	4.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	14.94	15.24	15.54
D	36.5	36.7	36.9
E	12.85	13.0	13.15
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b_p	0.35	0.45	0.55
b_2	0.63	0.73	1.03
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

REVISION HISTORY	7534 Group DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 18, 2000	–	First edition issued
1.10	Jun. 14, 2000	2	package type revised; 32P6B-A → 32P6U-A
		5	package type revised; 32P6B-A → 32P6U-A
		8	package type revised; 32P6B-A → 32P6U-A
		34	Description revised; $\overline{\text{RESET}}$ "L" pulse width 2 μs → 15 μs
		43	Table 11 revised; Absolute accuracy (excluding quantization error) → Linearity error
		44	Table 12 revised; tw($\overline{\text{RESET}}$): 2 → 15
		48	Fig. 51 Description ①, ② revised
		49	Fig. 52 Description ①, ② and package type revised; 32P6B-A → 32P6U-A
		50	Fig. 53 Description ①, ② revised
		51	Package outline revised; 32P6B-A → 32P6U-A
1.20	Sep. 5, 2000	34	Character fonts errors revised
1.30	Sep. 15, 2001	All pages	The following caution is eliminated; "PRELIMINARY Notice: This is not a final specification. Some parametric limits are subject to change."
		7	Table 1 Function description of V_{SS}, V_{CC} revised.
		8	Fig. 7 "M37534E4" added, "Under development" eliminated. Table 2 M37534E4GP added.
		9	"Note on stack page" added.
		15	Fig. 15 Ports $P3_6$, $P3_7$ revised.
		23	Description revised; 5 sources → 6 sources, "setup token receive" added.
		29	μ sec. → μs
		38	NOTES ON PROGRAMMING "Note on Stack Page" added. Handling of Power Source Pin; 0.1 μF → 1.0 μF, a ceramic capacitor → an electrolytic or a ceramic capacitor Handling of $USBVREF_{OUT}$ Pin; 0.1 μF → 0.22 μF
		39	DATA REQUIRED FOR MASK ORDERS revised. Table 6 32P6U-A added. Name of Programming Adapter revised.
		40	Note 3 revised.
		46	Table 14 7532 Group → 7532/7536 Group
2.00	Jun. 21, 2004	All pages	Words standardized: On-chip oscillator, A/D converter
		38	Electric Characteristic Difference Among Mask ROM and One Time PROM Version MCUs added.
		39	Note on Power Source Voltage added. DATA REQUIRED FOR MASK ORDERS revised.
		51	32P6U-A revised.
3.00	Oct. 23, 2006	All pages	Package names "36P2R-A" → "PRSP0036GA-A" revised Package names "32P6U-A" → "PLQP0032GB-A" revised Package names "42P4B" → "PRDP0042BA-A" revised "USB Spec. Rev.1.1" → "Low-Speed USB2.0 specification" revised
		36	Clock Generating Circuit; "No external resistor is needed .... resistor exists on-chip." → "No external resistor is needed .... depending on conditions.) Fig. 43; Pulled up added, NOTE added Fig. 46; NOTE 2 added
		38	NOTES ON PROGRAMMING; Watchdog Timer added NOTES ON USE; USB Communication added

Rev.	Date	Description	
		Page	Summary
3.00	Oct. 23, 2006	39 51, 52	NOTES ON USE; Note on A/D Converter added PACKAGE OUTLINE revised

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